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A Low Voltage Low Power CMOS Implementation of Second Generation Orderly Current Buffer

S. J. Azhari*(C.A.) and M. Zareie*

Abstract: In this paper, a novel low voltage low power current buffer was presented. The proposed structure was implemented in CMOS technology and is the second generation of OCB (orderly current buffer) called OCBII. This generation is arranged in single input-single output configuration and has modular structure. It is theoretically analyzed and the formulae of its most important parameters are derived. Pre and Post-layout plus Monte Carlo simulations were performed under ±0.75 V by Cadence using TSMC 0.18 µm CMOS technology parameters up to 3rd order. The proposed structure could expand and act as a dual output buffer in which the second output shows extremely high impedance because of its cascode configuration. The results prove that OCBII makes it possible to achieve very low values of input impedance under low supply voltages and low power dissipation. The most important parameters of 1st, 2nd and 3rd orders, i.e. input impedance (R_{in}), -3 dB bandwidth (BW), power dissipation (P_d) and output impedance (R_o) were found respectively in Pre-layout plus Monte Carlo results as:
1st order: R_{in} (52.4 Ω), BW (733.7 MHz), P_d (225.6 µW), R_o (105.6 kΩ)
2nd order: R_{in} (3.8 Ω), BW (576.4 MHz), P_d (307 µW), R_o (106.4 kΩ)
3rd order: R_{in} (0.34 Ω), BW (566.9 MHz), P_d (535.6 µW), R_o (118.2 kΩ)
And in Post-layout plus Monte Carlo results as:
1st order: R_{in} (59.9 Ω), BW (609.6 MHz), P_d (212.4 µW), R_o (106.9 kΩ)
2nd order: R_{in} (11.3 Ω), BW (529.3 MHz), P_d (389.9 µW), R_o (109.8 kΩ)
3rd order: R_{in} (5.8 Ω), BW (526.5 MHz), P_d (514.5 µW), R_o (125.5 kΩ)
Corner cases simulation results are also provided indicating well PVT insensitivity advantage of the block.

Keywords: Second Generation OCB, Current Buffer, Extremely Low Input Impedance, Very Wide Bandwidth Current Buffer, Current Mode.

1 Introduction

THE current mode approach of analog circuit design has recently gained considerable attention. High slew rate, high bandwidth, simple circuitry and low voltage operation are some of advantages of current mode circuits compared to voltage modes [1-8]. Current buffers are one of the main building blocks of current mode signal processors which find wide applications in realizing filters, oscillators, signal conditioners, current amplifiers etc. [9-18].

Current buffers are characterized by low input impedance ideally zero. The authors of [13] introduced, a novel type current buffer being called Orderly Current Buffer, OCB, which has the potential of producing low input impedance. The orderly current buffer have regular structure in which a core cell is repeated as many times as required to produce very low input impedance current buffers. The first generation of OCB called OCBI was implemented in fully differential structure in BJT technology [13]. The weakness of OCBI was its large power consumption which was reported as 10.3mW for 3rd order. In addition, due to the dominance of CMOS technology, implementing BJT type OCB may not be cost effective. To provide more

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structural flexibility and freedom the single ended arrangement is examined which shows excellent frequency operation and results in lower power consumption compared to OCBI. Favorably, the simple structure and lower power consumption of OCBII the implementation of its higher orders possible.

2 Circuit Analysis and Discussion

2.1 First Order Current Buffer (OCBII)

The circuitry of the 1st-order OCBII is shown in Fig.1. As it is seen an active feedback loop consisting of common gate input transistor M_1, current source I and gain transistor M_2 is such arranged that initially delivers most of I_{in} into the source node of M_1 (at input node, $r_{sM1}<<r_{oM2}$). It is then amplified by M_2 and fed back to the input node causing I_{in} to be mostly sunk by drain junction of M_2 rather than being sourced into source junction of M_1, at last. The input current which is such sunk by M_2 is mirrored to the buffer's output node by M_3. The order of the OCBII is taken after the number of the gain blocks of the feedback loop (i.e. M_2 here). The diode connected transistor M_D is used for appropriate level shifting.

$$C_1 \approx C_{dB_{M2}} + C_{gs_{M2}}$$
$$C_2 \approx C_{gs_{M1}}$$
$$C_3 \approx C_{gd_{M1}} + C_{db_{M1}} + C_{gs_{M2}} + C_{gs_{M3}} + 2C_{dg_{M2}} + 2C_{dg_{M3}} + C_1$$
$$C_4 \approx C_{dg_{M3}} + C_{db_{M3}}$$
$$R_B = R_{O_I} \left\| \left(R_{O_{I'}} + 1/g_{m_{MD}} \right) \approx R_{O_I} \right\| R_{O_{I'}} \quad (1)$$

In (1), g_m, C_I, C_{gs}, C_{db}, C_{dg}, r_O, R_{OI} and $R_{OI'}$ denotes the transconductance of the related transistor, output capacitance of current source I, gate-source capacitance, drain-body capacitance, drain-gate capacitance, output impedance of related transistor, output impedance of I current source and output impedance of I' current source respectively. The equivalent resistance of diode connected transistor D is also omitted for simplicity.
According to feedback theory we have:

$$Z_{\inf} = \frac{Z_{in}}{1+T} \quad (2)$$

where, Z_{in} is the open loop input impedance, T is the feedback loop gain and Z_{inf} is closed loop input impedance. By ignoring higher order poles and zeroes, the loop gain T can be found from:

$$T = \frac{I_f}{I_{in}} \approx \frac{r_{o_{M2}}}{r_{o_{M2}} + 1/g_{mM1}} \times R_B \times g_{m_{M2}} \times \frac{1}{1+sC_3R_B}$$
$$= \frac{K_1}{\left(1+\frac{S}{P_1}\right)} \quad (3)$$

while

$$K_1 = \frac{r_{o_{M2}}}{r_{o_{M2}} + 1/g_{m_{M1}}} \times R_B \times g_{m_{M2}} \quad (3.1)$$

$$P_1 = \left[R_B.C_3\right]^{-1} \quad (3.2)$$

Referring to (3) through (3.2), P_1 is the dominant pole of T and K_1 is the DC value of loop gain.

Z_{in} (open loop input impedance) and Z_{inf} (closed loop one) can be found as:

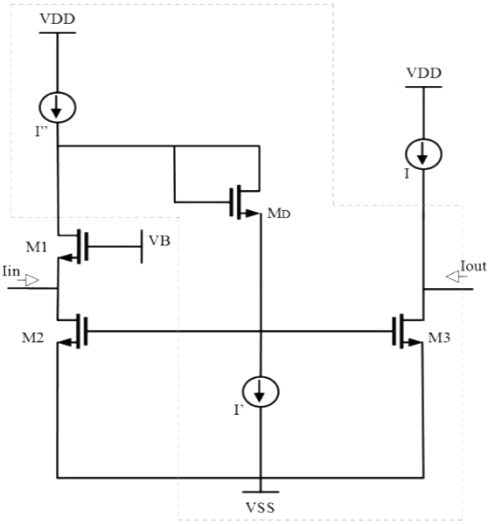


Fig. 1 1st order OCBII.

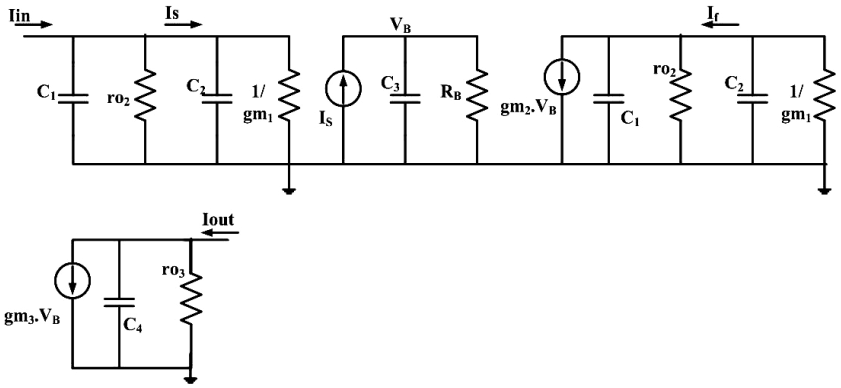


Fig. 2 Open loop small signal equivalent circuit of 1st order OCBII.

$$Z_{in} = \frac{1}{g_{m_{M1}}} \times \frac{1}{1+\frac{S}{P_2}} \tag{4}$$

$$P_2 = \left(\frac{1}{g_{m_{M1}}} \times (C_1 + C_2) \right)^{-1} \tag{4.1}$$

$$(Z_{in})_f = \frac{Z_{in}}{1+T} = \frac{1}{K_1 g_{m_{M1}}} \times \frac{1}{\left(1+\frac{S}{P_2}\right)} \times \frac{1+\frac{S}{P_1}}{\left(1+\frac{S}{K_1 P_1}\right)} \tag{5}$$

As it is seen from (5), Z_{inf} has a zero equal to the dominant pole of T in (3) and two much larger poles. On the other hand, the DC value of Z_{inf} is K_1 times lower than that of a simple common gate structure (i.e. $1/g_{mM1}$) with a very wide bandwidth (here in worst case, P_1) depending on the utilized transistors.

Now for A_{if}, using the feedback theory gives:

$$(Z_{in})_f = \frac{Z_{in}}{1+T} = \frac{1}{K_1 g_{m_{M1}}} \times \frac{1}{\left(1+\frac{S}{P_2}\right)} \times \frac{1+\frac{S}{P_1}}{\left(1+\frac{S}{K_1 P_1}\right)} \tag{6}$$

Eq. (6) shows that the DC value of A_{if} is close to unity while its bandwidth is:

$$BW = K_1 P_1 \tag{6.1}$$

Multiple output version of 1st order OCBII can also be simply implemented. Fig. 3 shows the two output version of OCBII. The first output is composed of simple current mirror with moderately high output impedance while the second output is composed of cascode current mirror exhibiting very high output impedance.

2.2 Higher Orders Structure (OCBII)

The repeating part of higher orders is common source arrangement as is shown in Fig. 4 in which M_{Nni} provides high loop gain and PMOS current mirror composed of M_{Pni}-M_{Pnii} simply transfer currents to the next stages. In the gain transistor, *N* indicates the type of transistor, i.e. NMOS, the index *n* is determined by the order of current buffer and *i* is the transistors' number. For the current mirror transistors, index *P* represents the type of transistor, i.e. PMOS, indexes *n* and *i* represents buffers order and transistors number, respectively. The first order is preceded by 2nd order as is shown in Fig. 5(a) which is implemented by adding one repeating part to the first order structure. As can be seen, *n* is replaced by 2 indicating the order of current buffer. In OCBII, the order of the buffer simply indicates the number of the used repeating part. Based on this discussion, the circuitry of 4th order of OCBII is shown in Fig. 5(b).

The open loop gain of the n^{th} order OCBII can be found as:

$$T \approx \frac{r_{o_{M2}}}{r_{o_{M2}} + 1/g_{m_{M1}}} \times \left(g_{m_{Ni}} \times R_B\right)^n \times \frac{1}{\left(1+\frac{S}{P_1}\right)\left(1+\frac{S}{P_3}\right)^{n-1}\left(1+\frac{S}{P_4}\right)^{n-1}} \tag{7}$$

$$P_3 = \left[\left(R_{O_I} r_{o_{Pnii}}\right) \times \left(C_{db_{MPnii}} + C_{dg_{Pnii}} + C_{gs_{Mni}} + 2 \times C_{dg_{Mni}}\right) \right]^{-1} \tag{7.1}$$

$$P_4 = \left[\frac{1}{g_{m_{Pni}}} \times \left(C_{gs_{Mpni}} + C_{gs_{Mpni}} + C_{db_{MNni}} + C_{db_{Mpni}} + C_{dg_{MNni}} + A \times C_{gd_{MPnii}}\right) \right]^{-1} \tag{7.2}$$

In (7.2), A is the miller effect on the drain gate capacitance of M_{Pnii} transistor and is defined as:

$$A = g_{m_{MPnii}} \times \left(r_{o_{MPnii}} \parallel R_{O_I}\right) \tag{7.3}$$

In frequency domain each repeating cell adds two poles to the 1st order structure according to (7). One of the extra poles is produced by gain transistor and the other is related to current mirror.

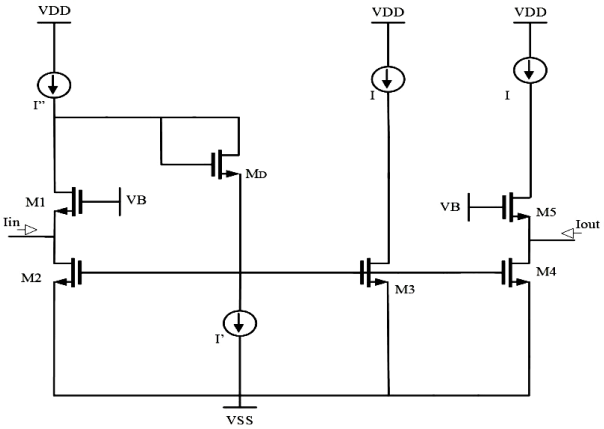


Fig. 3 Multiple output version of OCBII.

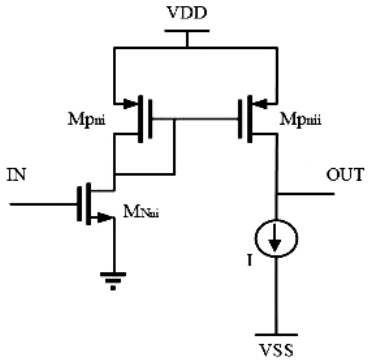


Fig. 4 Common source arrangement as the repeating part of higher orders.

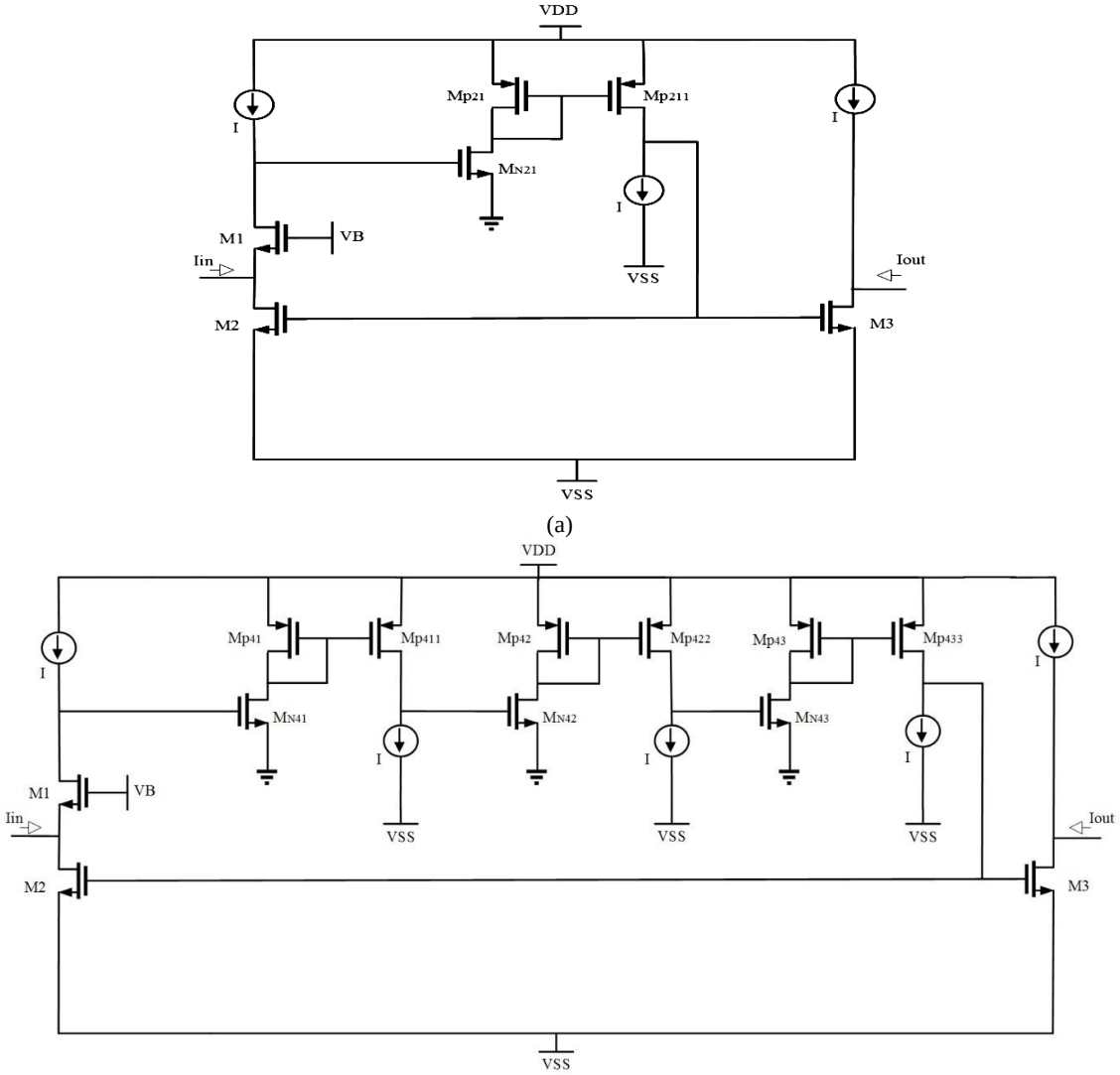


Fig. 5 Higher order OCBII; a) 2nd order and b) 4th order.

2.3 Higher Orders Compensation

As is done in OCBII, the higher order compensation is done by connecting compensation capacitor between input node and node B according to the block diagram of Fig. 6 in which R_B is the equivalent resistant of node B. In Fig. 6 we have:

$$T_1 = \frac{K_n'}{\left(1+\frac{S}{P_3}\right)^{n-1}\left(1+\frac{S}{P_4}\right)^{n-2}}$$

$$K_n' = \frac{r_{O_{M2}}}{r_{o_{M2}} + 1/g_{m_{M1}}} \times \left(g_{m_{M1}} \times R_B\right)^{n-1}$$

$$T_2 \approx \frac{K}{\left(1+\frac{S}{P_1}\right)\left(1+\frac{S}{P_4}\right)}$$

$$K = R_B g_{m_{M2}} \tag{8}$$

Using the block diagram of Fig. 6 it can be proved that the loop gain after compensation is:

$$A_{id} = \frac{T_1\left(1+SR_M C_M\right)}{S^2 \frac{C_M r_e}{P_2} + ST_1 C_M r_e + 1} \times T_2 \tag{9}$$

The open loop transfer function of (9) can be simplified to:

$$A_{id} = \frac{K_n' \times K}{\left(1+\frac{S}{P_d}\right)\left(1+\frac{S}{P_{nd}}\right)^{2n-1}} \tag{10}$$

where

$$P_d = \left(K_n' \times C_M \times \frac{1}{g_{m_{M1}}}\right)^{-1} \tag{10.1}$$

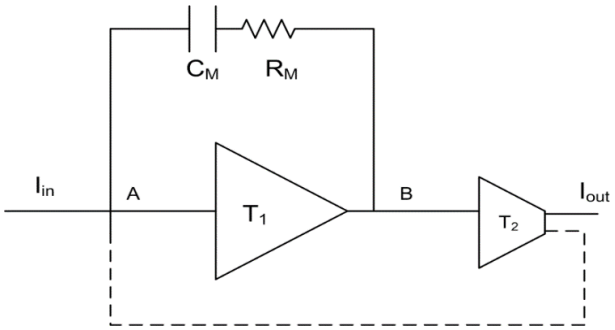


Fig. 6 Higher order block diagram after compensation.

$$\left|P_{nd}\right| = \sqrt[2n-1]{K_n' \times P_1 \times P_2 \times P_3^{n-1} \times P_4^{n-2}} \tag{10.2}$$

The dominant pole is much smaller than the non-dominant ones resulting in a proper phase margin. However the value of compensation capacitor is chosen such that the unity gain frequency of (10) gets smaller than non-dominant poles.

The open loop input impedance can also be found from (11).

2.4 Closed Loop Parameters of Higher Orders

Using (8)-(11), the closed loop parameters are found as follows:

$$A_{idf} \approx \frac{KK_n'}{\left(1+KK_n'\right)} \times \frac{1}{\left(1+\frac{S}{P_{df}}\right)^{2n}} \tag{12}$$

$$P_{df} = \sqrt[2n]{P_d \times P_{nd}^{2n-1}} \tag{12.1}$$

$$R_{id_f} = \frac{1}{\left(1+KK_n'\right) g_{m_{Q1}}} \times \frac{\left(1+SR_M C_M\right) \times \left(1+\frac{S}{P_3}\right)^{n-1} \times \left(1+\frac{S}{P_4}\right)^{n-2}}{\left(1+\frac{S}{P_{df}}\right)^{2n}} \tag{13}$$

3 Simulation Results and Discussion

To study the practical behavior of the block it is simulated up to 3th order for the single output configuration and the dual one. Both pre and post-Layout plus Monte Carlo (with 100 number of runs under mismatch and process variation) simulations are carried out by Cadence using TSMC 0.18 µm CMOS technology parameters under ±0.75 V supply voltage. The aspect ratios of transistors and the used element values are given in Tables 1 and 2, respectively.

Table 1 Transistor aspect ratio of the proposed circuit.

	Transistors	W[µm]/L[µm]
Non-Repeated Ones	M_1	80/0.5
	M_2,M_3	16/0.4
	M_D	30/0.18
	M_4	17.1/0.4
	M_5	17.1/0.18
Repeated Ones	M_{Nni}	60/0.18
	M_{Pni},M_{Pnii}	30.51/0.18

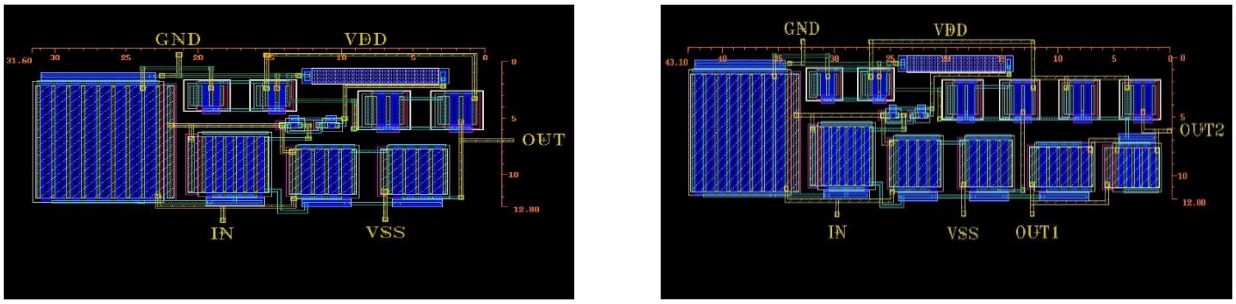
Table 1 The used elements' values.

Element		Value
I		30 [µA]
I'		20 [µA]
I''		50 [µA]
V_{DD} & V_{SS}		±0.75 [V]
V_B		0 [V]
C_M	1st	Not Required
	2nd	130 [fF]
	3rd	500 [fF]

The layout views of the OCBII are shown for the single output and dual output of the 1st order in Fig. 7, of the 2nd order in Fig. 8, and of the 3rd order in Fig.9. The proper frequency performance for a versatile current buffer defined as it shows low input impedance to wide bandwidth frequency input signals with low power consumption. The dual output structure show more output impedance from the cascode current mirror with the same input impedance as the single output structure. It only consumes a bit more power (about 70 µW as a mean value for the 1st, 2nd and 3rd orders) than the single output structure and also shows a wide bandwidth. The figures containing frequency bandwidth are responses of the single output design as the main structure.

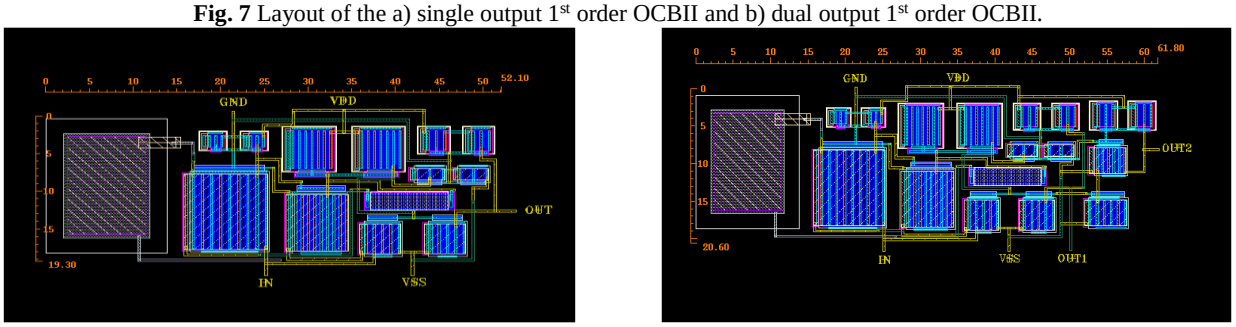
The stimulated frequency performance of the input impedances are 51.5 Ω, 3.2 Ω and 0.25 Ω for the 1st, 2nd and 3rd orders, respectively, and shown in Fig. 10. The Pre-layout plus Monte Carlo input impedances of 1st, 2nd and 3rd order OCBII are respectively shown as 52.4 Ω, 3.8 Ω and 0.34 Ω in Figs. 11(a)-(c), respectively. The post-layout plus Monte Carlo results of input impedances are also shown in Figs. 12(a)-(c), which are 59.5 Ω, 11.38 Ω and 5.8 Ω for the 1st, 2nd and 3rd orders, respectively.

$$R_{id} = \frac{1}{g_{m_{M1}}} \times \frac{\left(1+S.R_M C_M\right) \times \left(1+\frac{S}{P_3}\right)^{n-1} \times \left(1+\frac{S}{P_4}\right)^{n-2}}{S^2 \frac{C_M r_e}{P_2}\left(1+\frac{S}{P_1}\right)\left(1+\frac{S}{P_3}\right)^{n-1}\left(1+\frac{S}{P_4}\right)^{n-2} + SK_n' C_M r_e + \left(1+\frac{S}{P_1}\right)\left(1+\frac{S}{P_3}\right)^{n-1}\left(1+\frac{S}{P_4}\right)^{n-2}} \tag{11}$$



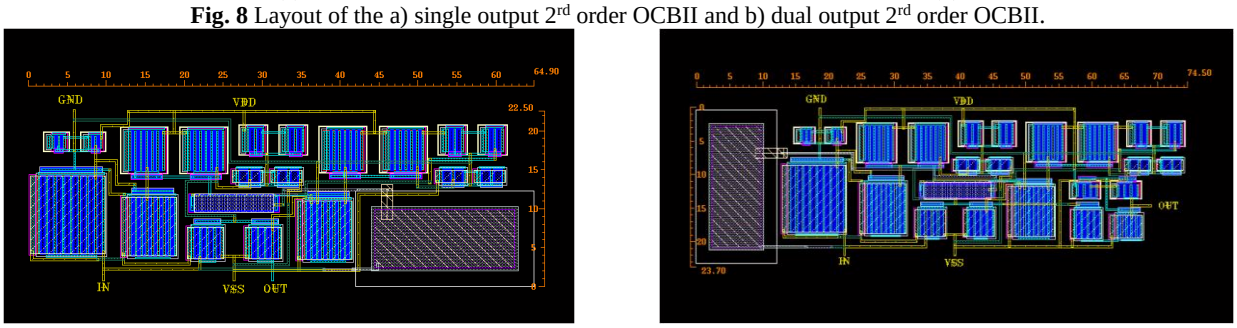
(a) (b)

Fig. 7 Layout of the a) single output 1st order OCBII and b) dual output 1st order OCBII.



(a) (b)

Fig. 8 Layout of the a) single output 2rd order OCBII and b) dual output 2rd order OCBII.



(a) (b)

Fig. 9 Layout of the a) single output 3rd order OCBII and b) dual output 3rd order OCBII.

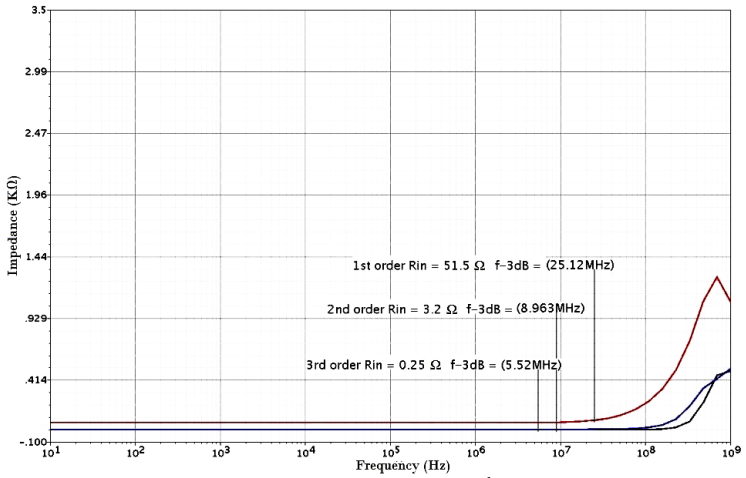


Fig. 10 Simulated R_{in} of the 1st to 3rd order OCBII.

Fig. 13 shows the excellent frequency performance of the unity gain A_i with 737 MHz, 581.9 MHz and 572 MHz, -3 dB bandwidths for the 1st, 2nd and 3rd orders in simulations results. Pre-layout plus Monte Carlo with bandwidth of 733.7 MHz, 576.4 MHz and 567.4 MHz for 1st, 2nd and 3rd order shows proper robustness to process variations and non-idealities. These results are also shown in Figs. 14(a)-(c), respectively.

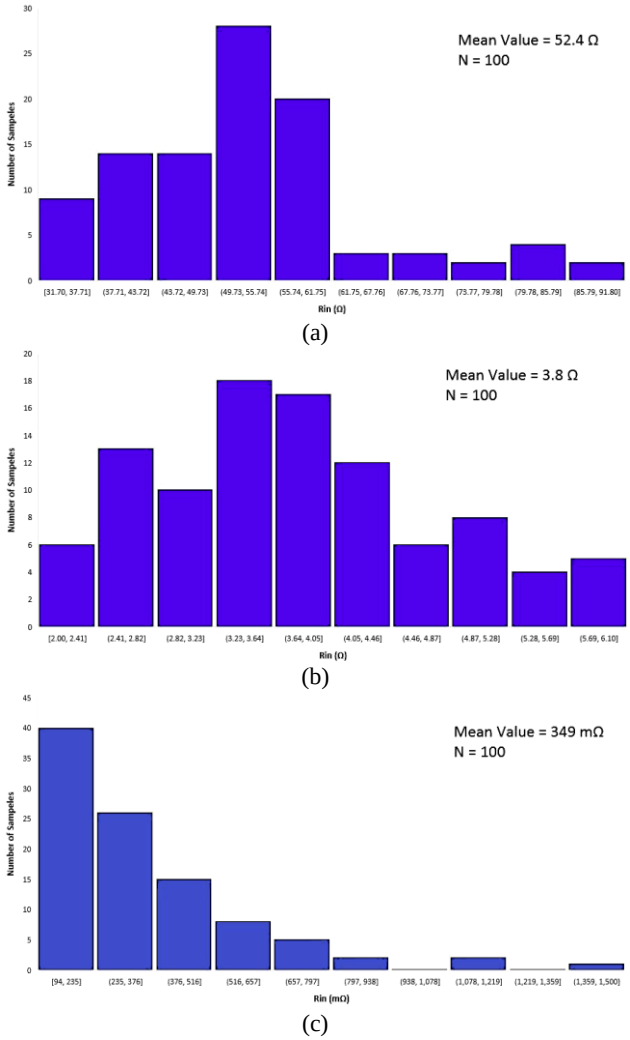


Fig. 11 Pre-layout plus Monte Carlo results of a) 1st order R_{in}, b) 2nd order R_{in}, and c) 3rd order R_{in}.

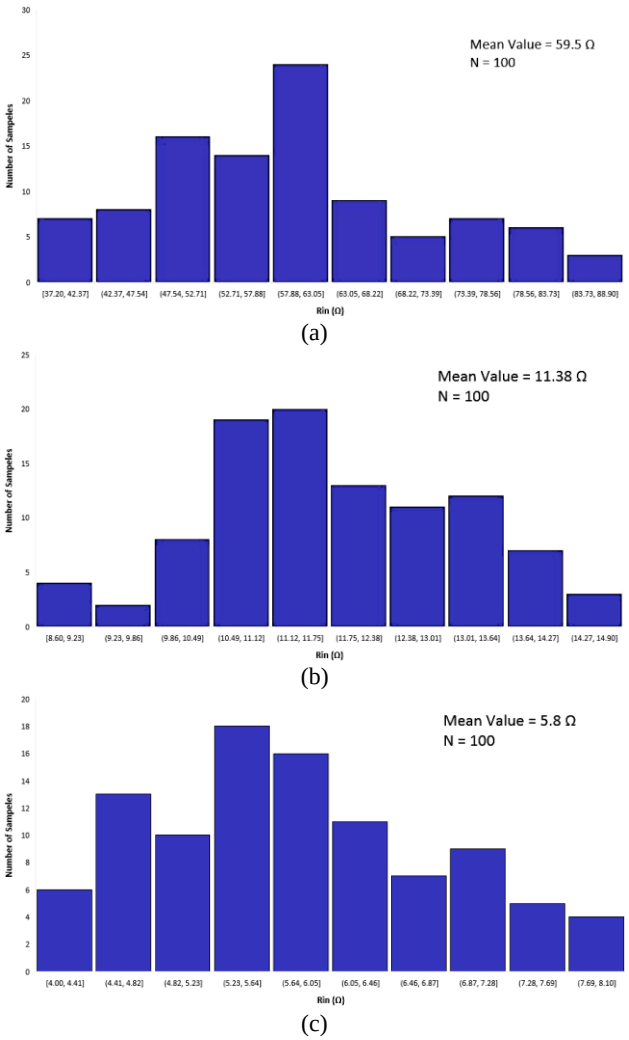


Fig. 12 Post-layout plus Monte Carlo results of a) 1st order R_{in}, b) 2nd order R_{in}, and c) 3rd order R_{in}.

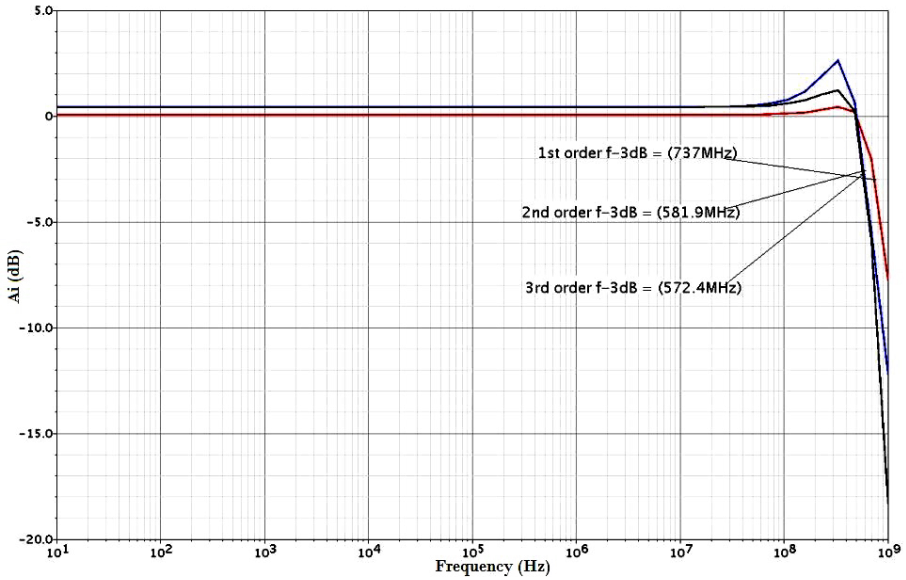
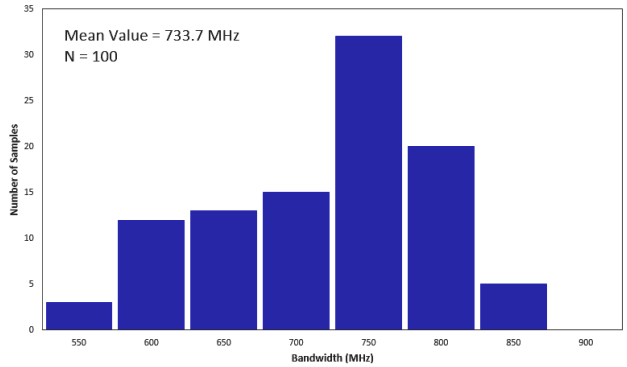
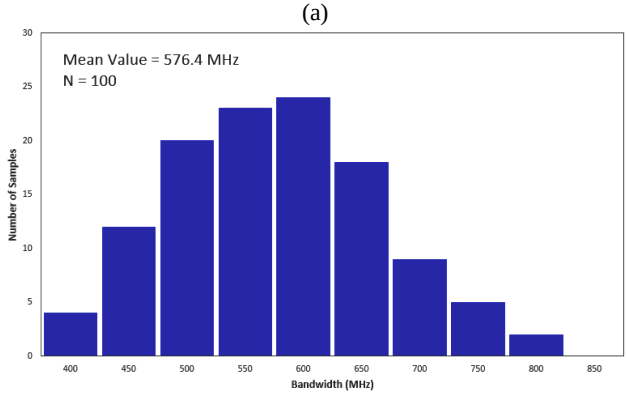


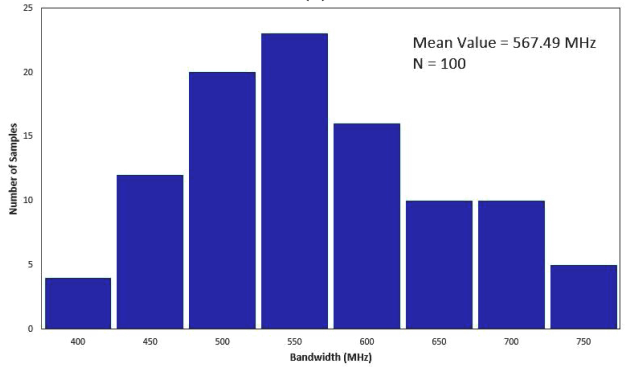
Fig. 13 A_i frequency performance in simulation results of 1st to 3rd order OCBII.



(a)

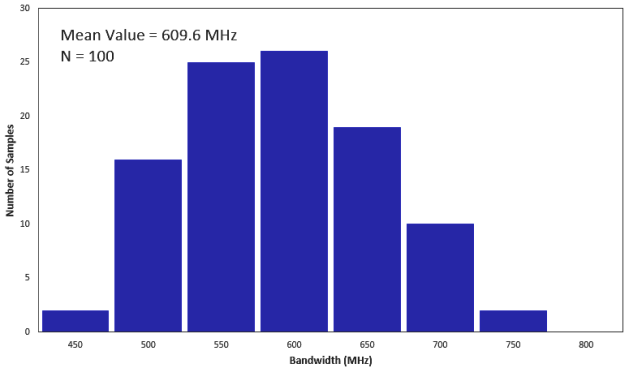


(b)

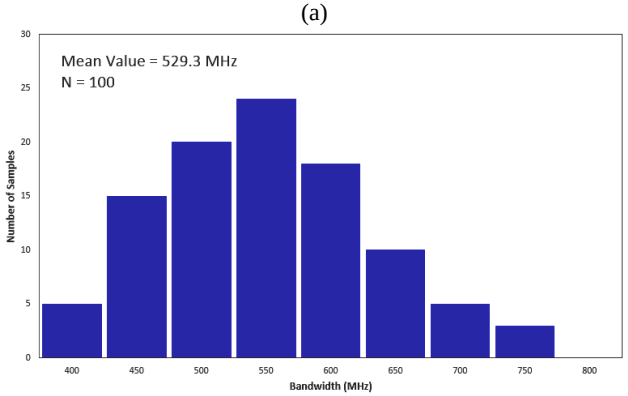


(c)

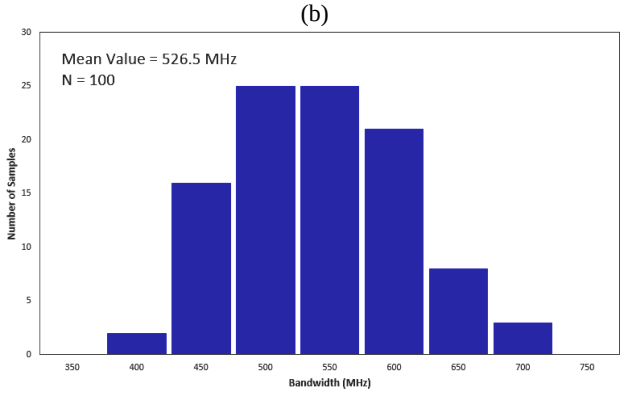
Fig. 14 Pre-layout plus Monte Carlo results of a) 1st order -3 dB BW, b) 2nd order -3 dB BW, and c) 3rd order -3 dB BW.



(a)



(b)



(c)

Fig. 15 Post-layout plus Monte Carlo results of a) 1st order -3 dB BW, b) 2nd order -3 dB BW, and c) 3rd order -3 dB BW.

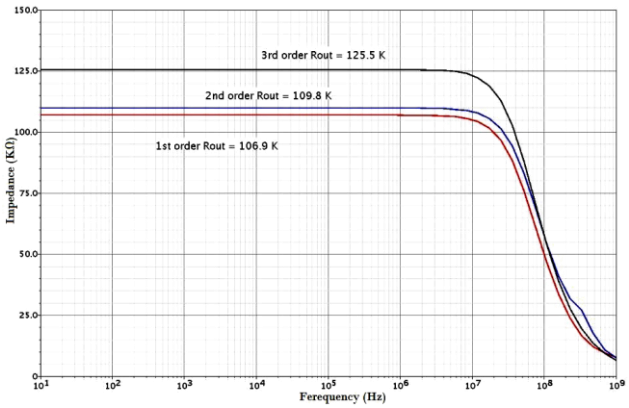


Fig. 16 The post-layout result of single output impedance of 1st to 3rd order OCBII.

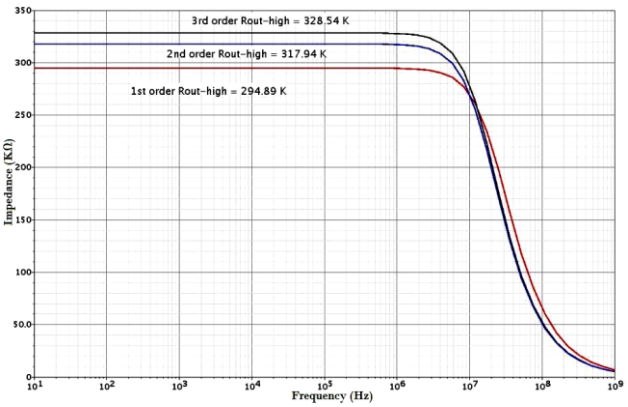
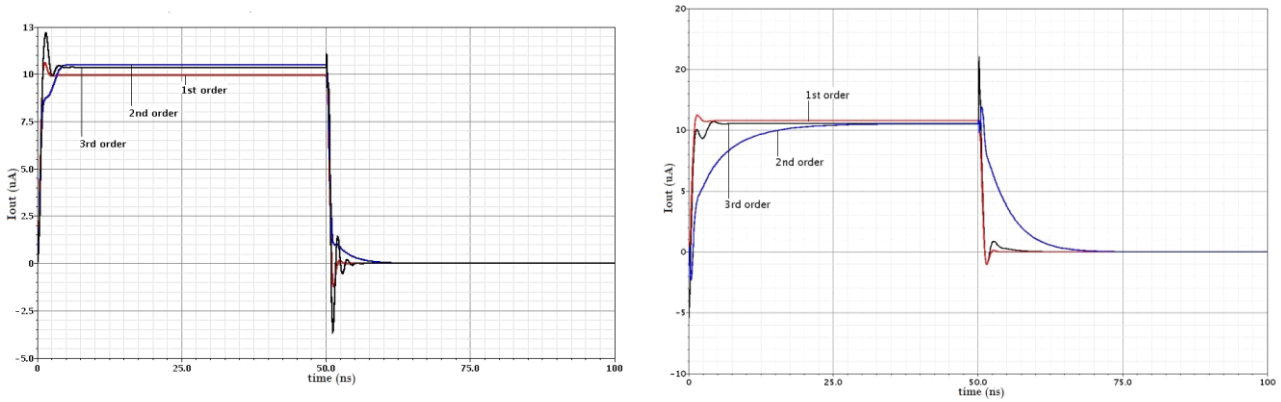


Fig. 17 The post-layout result of the high-output impedance structure of 1st to 3rd order OCBII.



(a) (b)

Fig. 18 a) Simulated step response of 1st to 3rd order OCBII and b) Post-layouted step response of 1st to 3rd order OCBII.

Table 3 Post-layout corner case simulation results of 1st to 3rd orders of OCBI.

Process Corners		TT	FF	SS	FS	SF
Temperature [°C]		27	-25	75	50	0
Supply Voltage [V]		±0.75	±0.825	±0.675	±0.75	±0.75
OCBII First Order	BW [MHz]	616.6	1370	255.13	403.9	776
	R_{in} [Ω]	58.6	27.4	138.6	56.6	68.2
OCBII Second Order	BW [MHz]	534.7	948.3	236.2	497.9	486.6
	R_{in} [Ω]	10.1	9.8	32.5	7.5	30.16
OCBII Third Order	BW [MHz]	530.1	896	221.1	474.8	480.9
	R_{in} [Ω]	5.1	4.06	15	5	10

Table 4 Comparison between the proposed OCBII with some related artworks.

Ref./Year		R_{in} [Ω]	f -3dB [MHz]	R_{out} [kΩ]	Power Consumption [mW]	Voltage Supply [V]	Number of Elements	FOM [MHz/μW]	Technology (CMOS) [μm]	Simulation
[14]/2016		18.33	4.5	700	0.051	1.8	[1]>>11	<<0.3×10^3	0.18	Simulation
[20]/2008		50	80	102	-	±0.75	[2]> 18	<0.4×10^2	0.18	Simulation
[21]/2013		3.7	450	127	1.02	±1.65	28	0.5×10^3	0.35	Simulation
[19]/2009		56.5	24.6	153	0.27[a]	±0.75	[2]> 18	<0.13×10^2	0.18	Post-Layout
[22]/2018		597	464.5	59	0.510[a]	±0.6	[2]> 12	<0.75×10	0.18	Post-Layout
Proposed[b]	1st	52.4	733.7	105.6	0.225	±0.75	11	0.6×10^3	0.18	Pre-Layout Plus Monte Carlo
	2nd	3.8	576.4	106.4	0.307	±0.75	14	0.38×10^4	0.18	
	3rd	0.34	566.9	118.2	0.535	±0.75	21	0.2×10^5	0.18	
	1st	59.9	609.6	106.9	0.212	±0.75	11	0.46×10^3	0.18	Post-Layout Plus Monte Carlo
	2nd	11.3	529.3	109.8	0.289	±0.75	14	0.12×10^4	0.18	
	3rd	5.8	526.5	125.5	0.514	±0.75	21	0.1×10^4	0.18	

[a] Calculated

[b] All of the results are related to single output structure.

[1] The self-biased current follower of [14] has an operational amplifier in its structure which the inner design of that was not available; so, it is not possible to find the exact number of elements.

[2] These blocks contain some current sources whose detailed structure are not available. To have a fair comparison, it is assumed that any current source made of only one transistor.

To validate the time domain response of the OCBII, its response to a step input with amplitude of 10 μA for 1st to 3rd orders are examined. The results for regular simulations and for the post-layout simulations are shown in Figs.18 (a) and 18(b), respectively which proves the OCBII's stability. Moreover, corner cases simulation after post-layout, for major parameters are also studied and reported in Table 3 which shows the robust performance of proposed current buffer.

Table 4 summarizes the performances of the second generation orderly current buffer and compares them to several recently reported works.

The comparison also includes the figure of merit (FOM) commonly used for current amplifiers performance comparison and defined as (14). However, one should take account into the fact that both of the pre

and post layout simulations in this work are plus Monte Carlo, while the related artworks did not define the impact of Monte Carlo simulations on the final results, so the high FOM results of OCBII shows the definite superiority of this work.

$$FOM \equiv \frac{R_{out} \times BW}{R_{in} \times Power \times Number\,of\ \ Elements} \tag{14}$$

To have a fair comparison, authors have considered the not-available parameter of related works as same as the values reported for the 1st order OCBII.

4 Conclusion

In this paper circuitries of 1st to 3rd orders are shown leading to the way of forming the second generation of OCBII in CMOS technology. It is formed in single input single output arrangement. The most important parameters of the proposed circuit are formulized and the merits are discussed. The simulations of the 1st to 3rd orders of OCBII are carried out by Cadence using 0.18 µm TSMC CMOS parameters. To evaluate the impact of PVT non-idealities on the presented work, the corner cases with temperature analysis and both the pre–layout and post-layout plus Monte-Carlo simulations are performed. Simulation results show that OCBII makes it possible to implement low power wide bandwidth current buffers with low input impedance by a simple structure.

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