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Cascaded Multilevel Inverter Based on Quasi-Z-Source Converter: Analysis, Design and Study of Optimal Structures

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Abstract: In this paper, a new topology for cascaded multilevel inverter based on quasi-Z-source converter is proposed. In the proposed topology the magnitude of output DC voltage is not limited to the sum of magnitude of DC voltage sources. Moreover, the reliability of the circuit due to capability of short circuit by Z-source network is increased. The quasi-Z-source converter in different modes is analyzed and the voltage gain is obtained. Also, the values of quasi-Z-source network components are designed. In the proposed topology, the number of DC voltage sources, the number of switches, installation area and cost in comparison with conventional multilevel inverters are significantly reduced. Three algorithms to determine the magnitude of DC voltage sources are proposed. Then the optimal structures for the minimum number of switches and DC voltage sources to generate the maximum voltage levels are presented. Moreover, the control method for the proposed topology is described. To verify the performance of the proposed topology, simulation and experimental results of proposed topology are presented.

Keywords: Z-Source Converter, Quasi-Z-Source Converter, Multilevel Inverter, Shoot-Through, Optimization.

1 Introduction

IN recent years, multilevel inverters and Z-source converters are becoming more and more popular in industrial and residential applications [1-2]. For applications such as FACTS devices, big electrical drives and dynamic voltage restorers, multilevel inverters have been presented as static converters with high power [2-3]. The main advantage of multilevel inverters is using of low voltage power switches that reduces switching losses and voltage stress across power switches. Moreover, voltage steps with small value for output voltage that leads to high power quality, proper electromagnetic adaptability and small harmonic components [4-5]. Nowadays, high attention to multilevel converters leads to novel structures with a wide diversity of control methods [6-9]. Cascaded H-bridge (CHB), neutral point clamped (NPC) or diode clamped, and flying capacitor (FC) or capacitor clamped are three basic types of multilevel inverters [10-11]. There are three different basic multilevel inverters: neutral point clamped (NPC) or diode clamped, flying capacitor (FC) or capacitor clamped, and cascaded H-bridge (CHB) [10-11]. Among these topologies, the CHB topologies are appropriate approach for applications with high voltage with regards to easiness of control [12] but high number of separated voltage sources in the topologies is needed. In [13-16], novel topologies have been introduced to decrease the number of used dc voltage sources for applications with high voltage.

In the conventional DC/ac systems an extra converter such as DC-DC boost chopper is used to increase the DC input voltage. In the proposed topology instead of using DC-DC boost chopper, quasi-Z-source converter is used that has advantages such as continuous input current, common ground, and low stress voltage [17]. Quasi-Z-source converter uses an impedance network between DC voltage source and inverter [18]. Increasing the voltage provided by shoot-through (ST) state of converter that it is not possible with conventional inverter and conventional multilevel inverter [19]. In

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comparison with the conventional inverter, quasi-Z-source converter has lower costs, higher reliability, less complexity, and higher efficiency [20-21]. The quasi-Z source inverter (qZSI) based cascaded multilevel inverter (CMI) have been widely studied in PV power systems because of their excellent ability to handle DC source voltage's wide variations in single-stage power conversion [22]. Quasi-Z source CMI (qZS-CMI) combined advantages of qZSI and CMI in [23] for applications to PV power system.

In this paper, a new simple and modular topology for cascaded multilevel inverter based on quasi-Z-source inverter converter is proposed. Conventional multilevel inverters do not have high voltage gain but the combination of quasi-Z-source network and multilevel inverter has this feature. The proposed topology produces a large number of voltage levels with lower number of components and power switches. Also, the performance of quasi-Z-source converter used in proposed topology in different operating modes is evaluated and the values of Z-source network components are obtained. Three algorithms to calculate the magnitude of DC voltage sources are proposed. Finally, to show correct performance of the proposed topology, simulation and experimental results are provided.

2 Proposed Topology

Although after Z-source network, quasi-Z-source network is the simplest type of impedance networks but despite the simplicity, this network is very appropriate. In the quasi-Z-source network, current input is continuous and the range of changes for shoot-through duty cycle is wide. Other advantages of quasi-Z-source network are available in the literatures. Fig. 1 shows the power circuit of proposed topology for multilevel inverters based on quasi-Z-source converter, which consists of the basic unit and a full-bridge inverter. The basic unit has n DC voltage sources and n quasi-Z-source network. Each quasi-Z-source network by using two switches is connected to the output and can generate a positive or zero voltage level. Each switch which is shown in Fig. 1 consists of an insulated gate bipolar transistor (IGBT) with an antiparallel diode. A staircase waveform with positive voltage level is generated by the basic unit. The basic unit has output voltage which can be equal to each quasi-Z-source network or binary, ternary …, or n'nary combinations of quasi-Z-source network. Hence, the maximum number of steps of output voltage for v_o' is equal to 2^n-1. There is connection between output side of the basic unit and a full-bridge single-phase converter, which alternates the polarity of input voltage and helps to generate a staircase negative and positive waveform in output. In Table 1, the values of voltages v_o' and v_o are shown for different conditions of switches S_1, S_2, …, S_n, T_1, and T_2. According to this table, 2^{n+1}-1 different values is obtained for v_o.

Switch T_1 of proposed unit in Fig. 1 should withstand output voltage of unit but this unit is only a segment of proposed multilevel inverters with several units which is shown in Fig. 2. The output voltage of a unit in comparison with output voltage of multilevel inverter is low and due to advances in semiconductor industries, the switch T_1 can tolerate easily. The proposed multilevel inverter is constituted by a cascade connection of sub-multilevel inverters as shown in Fig. 2. The structure of the first, second, … and k-th basic units has $2n_1$, $2n_2$, …, and $2n_k$ switches, respectively. The full-bridge inverters generate both positive and negative voltages with stepped waveforms in the output. In the proposed cascaded multilevel inverter, the total output voltage is obtained from combination of output voltages of the sub-multilevel inverters as follows:

$$v_o = v_{o1} + v_{o2} + \cdots + v_{ok} \tag{1}$$

Combinations of switching states for every cell can lead to different levels of output voltage. By choosing

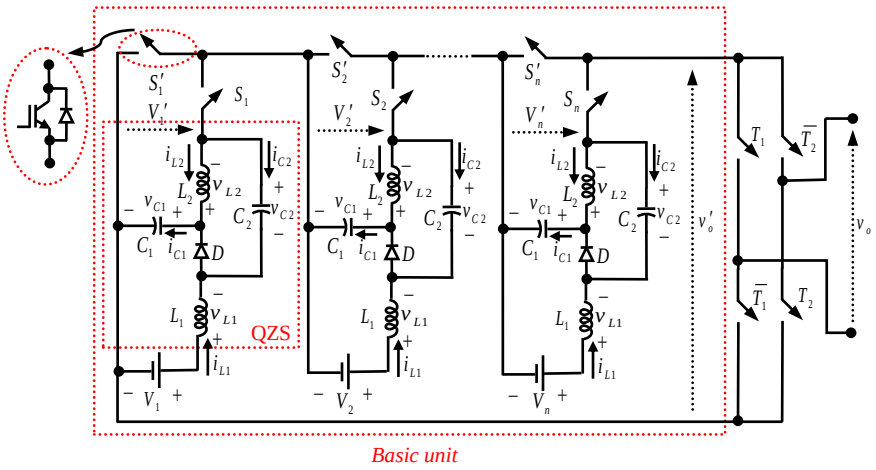

Fig. 1 Basic unit of proposed topology.

appropriate values for DC voltage sources, the output voltage of inverter is calculated between $\left(-\sum_{i=1}^{k}\sum_{j=1}^{n_i}V'_{ij}\right)$ and $\left(-\sum_{i=1}^{k}\sum_{j=1}^{n_i}V'_{ij}\right)$. By considering the number of DC voltage sources in basic cell equal to one, there is no requirement for transistors in basic cell. In the proposed topology, the generated output voltage by quasi-Z-source network is connected to the full-bridge inverter. In other words, this topology is equivalent to the CHB inverter with quasi-Z-source network. It is noticeable that quasi-Z-source network avoids from short-circuiting DC voltage sources. Due to this fact that there is no any DC voltage source with direct connection to back of un-folded H-bridge; so, short-circuiting a leg does not lead to short-circuit status of DC voltage sources. In fact, the proposed topology has been protected from short-circuiting DC voltage sources. If the designer and engineer do not consider the way to control input current, classic Z-source converter can lead to high inrush current at start-up. This issue is as result of charging the capacitors. The capacitors at start-up have low impedance against current. If the high value of current is not controlled, the value of current can be tens of amperes. There is a traditional method to decrease the value of inrush current and that method is using the combination of resistor and TRIAC or thermistor with negative thermal factor. Of course, there are other methods to control inrush current that can be founded in the papers. In the quasi-Z-source converters, value of inrush current is low in comparison with Z-source converters. The reason of low inrush current in the quasi-Z-source converters, use of inductor in series with input source.

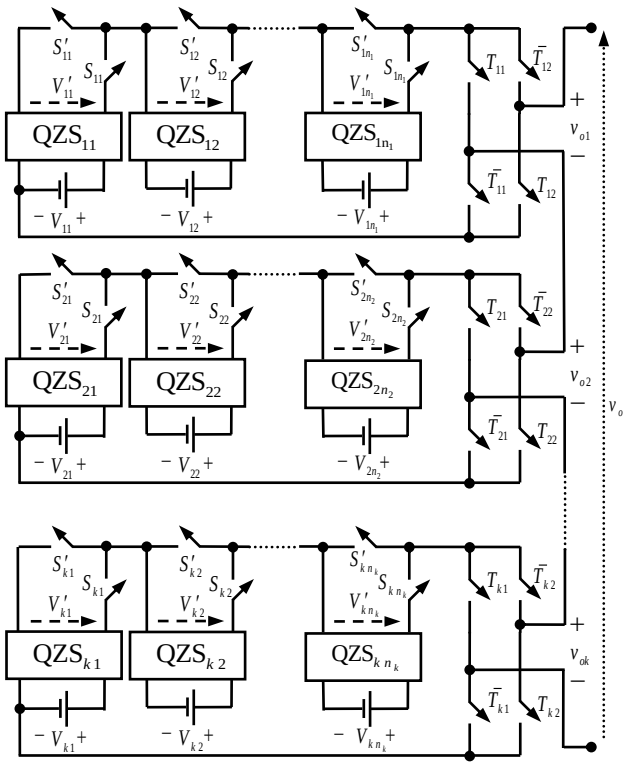

Fig. 2 Proposed multilevel inverter topology based on quasi-Z-source converter.

In each basic unit of the proposed topology as shown in Fig. 1, there are *n* quasi-Z-source networks. Each quasi-Z-source network is connected to the output by two switches. Fig. 3 shows the structure of quasi-Z-source converter that includes a DC voltage source and a quasi-Z-source network with two switches (S_1 and S'_1). In Fig. 3(a), the following assumptions are considered [24]:

$$L = L_1 = L_2 \tag{2}$$

$$C = C_1 = C_2 \tag{3}$$

The converter shown in Fig. 3(a) has two operating modes in continuous conduction mode (CCM). The first operating mode is ST state with T_{ST} period and the second operation mode is non-ST state with T_{nST} period that there is always the following equation [25]:

$$T_s = T_{ST} + T_{nST} \tag{4}$$

Duty cycle of ST mode (D_{ST}) is calculated as follows:

$$D_{ST} = \frac{T_{ST}}{T_s} \tag{5}$$

Duty cycle of non-ST mode is D_{nST} and is defined as follows:

$$D_{nST} = 1 - D_{ST} \tag{6}$$

Table 1 Values of v'_o and v_o for different conditions of switches.

State	Switches states						v'_o	v_o
	S_1	S_2	⋯	S_n	T_1	T_2		
1	off	off	⋯	off	on	off	0	0
2	on	off	⋯	off	off	off	V'_1	V'_1
3	on	off	⋯	off	on	on	V'_1	$-V'_1$
4	off	on	⋯	off	off	off	V'_2	V'_2
5	off	on	⋯	off	on	on	V'_2	$-V'_2$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2*n*	off	off	⋯	on	off	off	V'_n	V'_n
2*n*+1	off	off	⋯	on	on	on	V'_n	$-V'_n$
2*n*+2	on	on	⋯	off	off	off	$V'_1+V'_2$	$V'_1+V'_2$
2*n*+3	on	on	⋯	off	on	on	$V'_1+V'_2$	$-V'_1-V'_2$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2^{n+1}-4	on	on	⋯	off	off	off	$\sum_{i=1}^{n-1}V'_i$	$\sum_{i=1}^{n-1}V'_i$
2^{n+1}-3	on	on	⋯	off	on	on	$\sum_{i=1}^{n-1}V'_i$	$-\sum_{i=1}^{n-1}V'_i$
2^{n+1}-2	on	on	⋯	on	off	off	$\sum_{i=1}^{n}V'_i$	$\sum_{i=1}^{n}V'_i$
2^{n+1}-1	on	on	⋯	on	on	on	$\sum_{i=1}^{n}V'_i$	$-\sum_{i=1}^{n}V'_i$

The equivalent circuits of the converter is shown in Fig. 3(a) in the both operation modes are shown in Fig. 3.

2.1 First Operating Mode (ST Mode)

In this operating mode, both switches S_1 and S_1' are on that indicate ST state. In this mode, diode D is in reverse bias and off. The equivalent circuit of this operating mode is shown in Fig. 3(b). In this operating mode, by applying KVL in Fig. 3(b), the following equations are obtained:

$$v_{L1} = V_1 + V_{C2} \tag{7}$$

$$v_{L2} = V_{C1} \tag{8}$$

where V_{C1}, V_{C2}, and V_1 are average voltages across capacitors C_1, C_2, and DC voltage source, respectively. V_{L1} and V_{L1} are voltages across inductors L_1, and L_2, respectively.

In the first operating mode, the output voltage of Z-source network is zero.

2.2 Second Operating Mode (Non-ST Mode)

In this operating mode, S_1 or S_1' is on that indicate non-ST state. In this mode, diode D is conducting. The equivalent circuit of this operating mode is shown in Fig. 3(c). In this operating mode, by applying KVL in Fig. 3(c), the following equations are obtained:

$$v_{L1} = V_1 - V_{C1} \tag{9}$$

$$v_{L2} = -V_{C2} \tag{10}$$

In this mode, the output voltage of Z-source network is equal to maximum value. Maximum output voltage of Z-source network (V_1') is obtained from the following equation:

$$V_1' = V_{C1} + V_{C2} \tag{11}$$

2.2.1 Boost Factor of Quasi-Z-source Network

According to voltage balance law, the average voltage across an inductor is zero. Putting inductors L_1 and L_2 average voltage equal to zero, the following results are obtained:

$$V_{C1} = \frac{1 - D_{ST}}{1 - 2D_{ST}} V_1 \tag{12}$$

$$V_{C2} = \frac{D_{ST}}{1 - 2D_{ST}} V_1 \tag{13}$$

By substituting the values of V_{C1} and V_{C2} from (12) and (13) into (11), the maximum output voltage of quasi-Z-source is calculated as follows:

$$V_1' = \frac{1}{1 - 2D_{ST}} V_1 \tag{14}$$

Table 2 indicates the values of Z-source network output voltage for states of switches S_1 and S_1'.

2.2.2 Quasi-Z-Source Component Design

During ST state, the inductors voltage is positive and inductors currents increases linearly. The task of the inductor is to limit the current ripple during ST state [26]. The following equation is always valid:

$$v_L = L \frac{di_L}{dt} \tag{15}$$

Considering (8) and (15), equation between voltages across inductor and current through them in ST mode is obtained as follows:

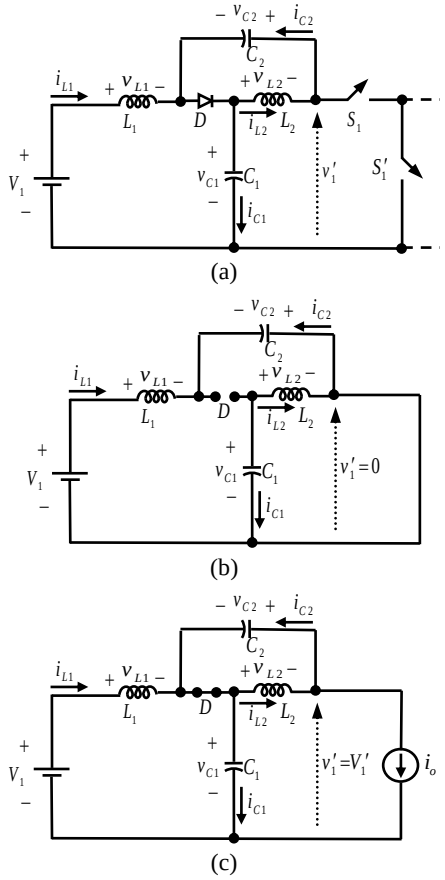

Fig. 3 Quasi-Z-source converter; a) Power circuit; b) Equivalent circuit in ST operation mode; and c) Equivalent circuit in non-ST operation mode.

Table 1 Switches states and Z-source network output voltage value.

State	Quasi-Z-Source Output Voltage	ON Switches
1	V_1' (non-ST)	S_1
2	0 (non-ST)	S_1'
3	0(-ST)	S_1, S_1'

$$L\frac{\Delta i_L}{D_{ST}T_s}=V_{C1} \tag{16}$$

In above equation, Δi_L is inductors current ripples.

Regarding to (16), the value of inductance is calculated as follows:

$$L=\frac{V_{C1}D_{ST}T_s}{\Delta i_L} \tag{17}$$

Considering $T_s=\frac{1}{f_s}$, the following result is obtained:

$$L=\frac{V_{C1}D_{ST}}{f_s\ \Delta i_L} \tag{18}$$

The capacitor absorbs the current ripple and achieves quite a stable voltage [27]. The inductor is charged by the capacitor during ST time. By applying KCL in Fig. 3(b), the following equation is obtained:

$$i_{C2}=-i_{L1} \tag{19}$$

where i_{L1} and i_{C2} are currents of L_1 and C_2, respectively.

The following equation is always valid:

$$i_C=C\frac{dv_C}{dt} \tag{20}$$

Consideration (19) and (20), the following result is obtained:

$$C\frac{\Delta v_C}{D_{ST}T_s}=I_L \tag{21}$$

In above equation, I_L is average currents through inductor and Δv_C is voltages ripples across capacitor.

Considering (21), the capacitor value is obtained as follows:

$$C=\frac{D_{ST}I_L}{f_s\ \Delta v_C} \tag{22}$$

3 Calculation of the Amplitudes of DC Voltage Sources

To generate output steps with high number without additional inverters, asymmetric topologies can be applied. An appropriate select of voltage asymmetry through cells can generate a various combination of voltage levels and delete redundancies. For the proposed structure, three different processes for designation of amplitudes of the DC voltage sources are presented.

3.1 First Proposed Strategy

In this strategy, the values of DC voltage sources in every cell are same. In the per-unit system, the base value is the first DC voltage source V_{11} and we have:

$$V_b=V_{11}=V_{dc} \tag{23}$$

To produce all steps in the output, the normalized values of DC voltage sources are written as follows:
First cell:

$$V_{1i}=V_{11}=V_{dc},\quad i=2,\cdots,n_1 \tag{24}$$

Second cell:

$$V_{1i}=V_{21}=V_{11}+2\sum_{j=1}^{n_1}V_{1j}=(2n_1+1)V_{dc},i=2,\cdots,n_2 \tag{25}$$

Third cell:

$$\begin{aligned}V_{3i}=V_{31}&=V_{11}+2\sum_{j=1}^{n_1}V_{1j}+2\sum_{j=1}^{n_2}V_{2j}\\&=(2n_1+1)(2n_2+1)V_{dc},\quad i=2,\cdots,n_3\end{aligned} \tag{26}$$

In general, for the *m*-th unit:

$$\begin{aligned}V_{mi}=V_{m1}&=V_{11}+2\sum_{j=1}^{m-1}\sum_{l=1}^{n_j}V_{jl}\\&=\prod_{j=1}^{m-1}(2n_j+1)V_{dc},\quad i=2,\cdots,n_m\end{aligned} \tag{27}$$

The maximum output voltage can be written as follows:

$$\begin{aligned}N_{step,1}&=\prod_{i=1}^{k}(2n_i+1)\\&=(2n_1+1)\times(2n_2+1)\times\cdots\times(2n_k+1)\end{aligned} \tag{28}$$

3.2 Second Proposed Strategy

In the second strategy, the normalized values for DC voltage sources in every cell are determined as follows:
First cell:

$$V_{11}=V_{dc} \tag{29}$$

$$V_{1i}=2V_{11}=2V_{dc},\quad i=2,\cdots,n_1 \tag{30}$$

Second cell:

$$V_{21}=V_{11}+2\sum_{i=1}^{n_1}V_{1i}=(4n_1-1)V_{dc},\quad i=2,\cdots,n_2 \tag{31}$$

In general, for the *m*-th cell:

$$V_{m1}=V_{11}+2\sum_{i=1}^{m-1}\sum_{j}^{n_i}V_{ij}=\prod_{i=1}^{m-1}(4n_i-1)V_{dc} \tag{32}$$

$$V_{mi}=2V_{m1}=2\prod_{j=1}^{m-1}(4n_j-1)V_{dc},\quad i=2,\cdots,n_m \tag{33}$$

In the following equation, the number of provided steps

in the output voltage is written:

$$N_{step,2} = \prod_{i=1}^{k} (4n_i - 1) \tag{34}$$

3.3 Third Proposed Strategy

To determine amplitudes of DC voltage sources in the third strategy, binary method in every cell is used that leads to an exponential increase in the number of total output steps.
In the *m*-th cell, the DC voltage sources are calculated as follows:

$$V_{m1} = V_{11} + 2\sum_{i=1}^{m-1}\sum_{j=1}^{n_i} V_{ij} = \prod_{i=1}^{m-1} (2^{n_i+1} - 1) V_{dc} \tag{35}$$

$$V_{mi} = 2^{i-1} V_{m1}, \qquad i = 2, \cdots, n_m \tag{36}$$

Determination of number of output voltage steps is as follows:

$$N_{step,3} = \prod_{i=1}^{k} (2^{n_i+1} - 1) \tag{37}$$

By selecting different values of duty ratio for quasi-Z-source network in the asymmetric conditions, it is possible to propose new strategies that lead to low number of elements. Due to application of proposed topology in photovoltaic systems, value of duty ratio is determined through maximum power tracking control system and as a result, availability to different values of duty ratio is difficult because these values depends on features and environmental conditions of photovoltaic cells.

4 Optimized Topologies

To generate specified number of levels in output voltage, different arrangement of proposed structure with different number of element can be used. In this section, optimized structures with different objectives for the proposed topology are investigated.

4.1 Optimized Topology With Constant Number of Switches to Achieve Maximum Number of Voltage Levels

The favorable goal in a multilevel converter is providing the high number of steps by using low number of switches. With constant consideration of number of switches (N_{switch}), determination of maximum number of steps for output voltage is necessary.

By considering a series of k sub-multilevel inverters for the proposed structure and n_i quasi-Z-source networks and n_i DC voltage sources for each of them (i = 1, 2, …, k), the following equation can be written:

$$N_{switch} = 2(n_1 + n_2 + \cdots + n_k) + 4k \tag{38}$$

The number of steps for voltages is obtained from (28), (34), and (37) for specification of DC voltage sources in three proposed strategy. By using these equations and (38), the maximized value for product of the numbers (whose summation is constant) is available when correctness of the following equation is acceptable:

$$n_1 = n_2 = \cdots = n_k = n \tag{39}$$

By substituting above equation in (38), the following result is obtained:

$$k = \frac{N_{switch}}{2n + 4} \tag{40}$$

The value of n must be determined and the number of switches N_{switch} is constant. By substituting (14) into (28), (34), and (37), the steps of voltage with maximum number for three strategies are obtained as follows, respectively:

$$N_{step,1} = (2n + 1)^k \tag{41}$$

$$N_{step,2} = (4n - 1)^k \tag{42}$$

$$N_{step,3} = (2^{n+1} - 1)^k \tag{43}$$

By substituting value of k from (40) into the above relations, following results are obtained:

$$N_{step,1} = \left[(2n + 1)^{\frac{1}{2n+4}} \right]^{N_{switch}} \tag{44}$$

$$N_{step,2} = \left[(4n - 1)^{\frac{1}{2n+4}} \right]^{N_{switch}} \tag{45}$$

$$N_{step,3} = \left[(2^{n+1} - 1)^{\frac{1}{2n+4}} \right]^{N_{switch}} \tag{46}$$

In Fig. 4(a), the changes of $(2^{n+1} - 1)^{\frac{1}{2n+4}}$, $(4n - 1)^{\frac{1}{2n+4}}$, and $(2n + 1)^{\frac{1}{2n+4}}$ against n are shown. It is obvious that for the 1st and 2nd strategies, the maximum number of steps for voltage is provided for n = 2. In other words, a topology with 2 quasi-Z-source networks, 2 DC voltage sources and 4 switches in every basic cell can generate maximum steps for v_o while minimum number of switches is used. In the 3rd strategy, the maximum steps of voltage is theoretically provided for $n = \infty$. In other words, for a constant number of switches a topology with one basic cell and available switches is favorable. It should be noticed that the number of elements is integer. Hence, if the number is not an integer, then the nearest integer is the answer to the problem.

4.2 Optimized Topology With Constant Number of Quasi-Z-Source Networks and DC Voltage Sources to Achieve Maximum Number of Voltage Levels

By considering unchangeable number of DC voltage

sources equal to N_{source}, the objective is finding a structure with capability of generating high number of voltage levels. By assuming that the proposed topology has a series of k sub-multilevel inverters, each of them has n_i DC voltage sources (for $i = 1, 2, \ldots, k$). Hence, we have:

$$N_{source} = \sum_{i=1}^{k} n_i = n_1 + n_2 + \cdots + n_k \tag{47}$$

In the following, the number of DC sources is calculated by using (39):

$$N_{source} = n \times k \tag{48}$$

By substituting the value of k from (48) into (41), (42), and (43), the maximum number of steps of voltage for three strategies is provided as follows:

$$N_{step,1} = \left[(2n+1)^{\frac{1}{n}} \right]^{N_{source}} \tag{49}$$

$$N_{step,2} = \left[(4n-1)^{\frac{1}{n}} \right]^{N_{source}} \tag{50}$$

$$N_{step,3} = \left[(2^{n+1}-1)^{\frac{1}{n}} \right]^{N_{source}} \tag{51}$$

In Fig. 4(b), the change of $(2^{n+1}-1)^{\frac{1}{n}}$, $(4n-1)^{\frac{1}{n}}$ and $(2n+1)^{\frac{1}{n}}$ against n is shown. It is obvious that the higher number of steps of voltage for 1st, 2nd, and 3rd strategies are achieved for $n = 1$. Hence, a topology has cells with one DC voltage source and one quasi-Z-source network generates high number of steps for v_o with low number of used DC sources. It is noticeable that the suggested structure is fundamentally a traditional cascaded multilevel inverter with one quasi-Z-source converter.

4.3 Optimized Topology for Constant Number of Steps of Voltage With Low Number of Power Switches

By considering the number of steps of voltage v_o equal to N_{step} and to generate steps of voltage, determination of structure with low number of switches is possible. This is obvious that in the basic cell, the high number of steps of voltage is provided for equal number of power switches. Hence, by considering (39)–(43) and the number of power switches in every cell equal to n, the total numbers of switches N_{switch} in the three strategies is calculated as follows:

$$N_{switch,1} = (2n+4)k = \ln\left(N_{step}\right) \times \frac{2n+4}{\ln(2n+1)} \tag{52}$$

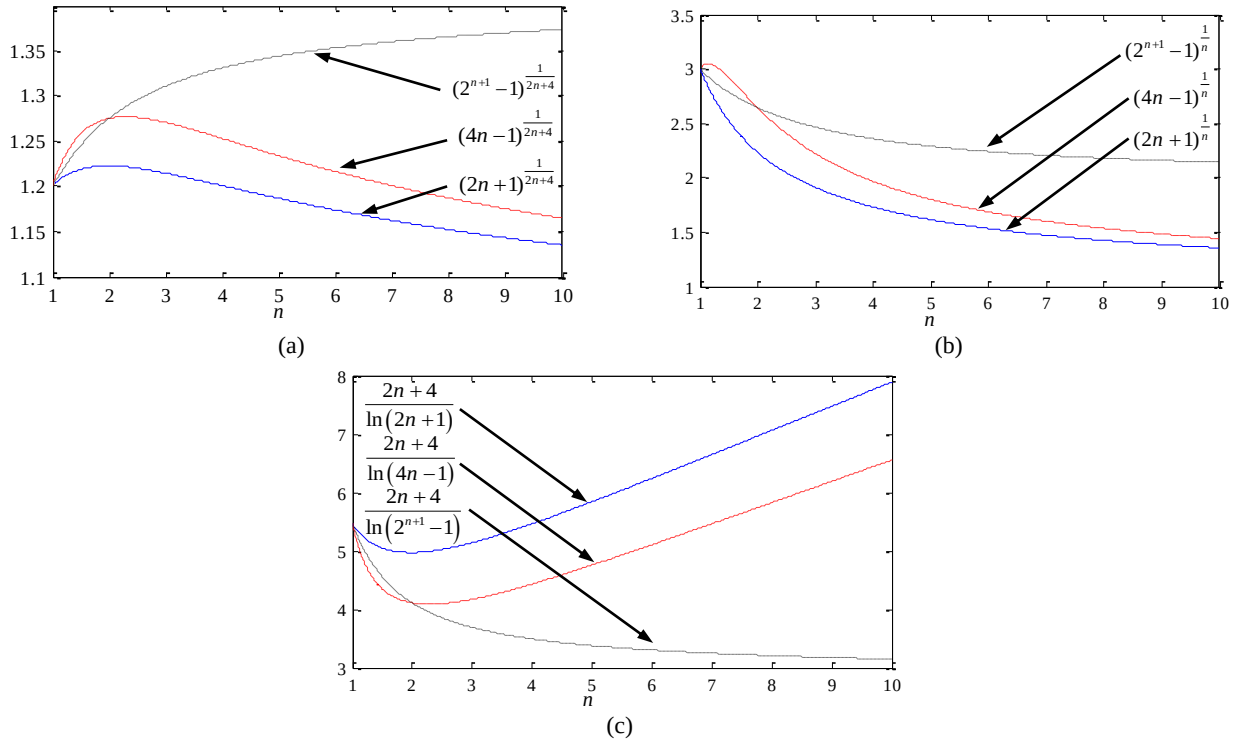

Fig. 4 a) Variation of $(2n+1)^{\frac{1}{2n+4}}$, $(4n-1)^{\frac{1}{2n+4}}$, and $(2^{n+1}-1)^{\frac{1}{2n+4}}$ versus n, b) Variation of $(2n+1)^{\frac{1}{n}}$, $(4n-1)^{\frac{1}{n}}$, and $(2^{n+1}-1)^{\frac{1}{n}}$ versus n, and c) Variation of $\frac{2n+4}{\ln(2n+1)}$, $\frac{2n+4}{\ln(4n-1)}$, and $\frac{2n+4}{\ln(2^{n+1}-1)}$ versus n.

$$N_{switch,2} = (2n+4)k = \ln\left(N_{step}\right) \times \frac{2n+4}{\ln\left(4n-1\right)} \quad (53)$$

$$N_{switch,3} = (2n+4)k = \ln\left(N_{step}\right) \times \frac{2n+4}{\ln\left(2^{n+1}-1\right)} \quad (54)$$

In Fig. 4(c), the change of $\frac{2n+4}{\ln\left(2n+1\right)}$, $\frac{2n+4}{\ln\left(4n-1\right)}$, and $\frac{2n+4}{\ln\left(2^{n+1}-1\right)}$ against n is shown. At the low point of presented shapes in Fig. 4(c) and for a constant value of N_{step}, the numbers of switches will be minimized. Hence, $n = 2$ is the lowest number of switches for achievement to N_{step} voltage levels in the 1st and 2nd strategies. In theory, the optimized amount for the 3rd strategy is achieved for $n = \infty$.

5 Control Method

There are many kinds of modulation methods for multilevel inverters [28-31]. The objective of some of them is minimization of total harmonic distortion and elimination of harmonics [32-33]. In this paper, the level-shifted sinusoidal pulse-width modulation (LS-SPWM) is used [34-35]. The general layout of this controlling method for producing various voltage levels is shown in Fig. 5(a), and the waveforms of the method for producing 5-level are shown in Fig. 5(b). Fig. 5(c) shows the control block diagram of the proposed structure. In this controlling method for producing N_{step} levels at the output voltage, N_{step}-1 triangular carrier wave with frequency f_s is considered. The reference signal (u_{ref}) is a sinusoidal waveform with frequency f_{ref}.

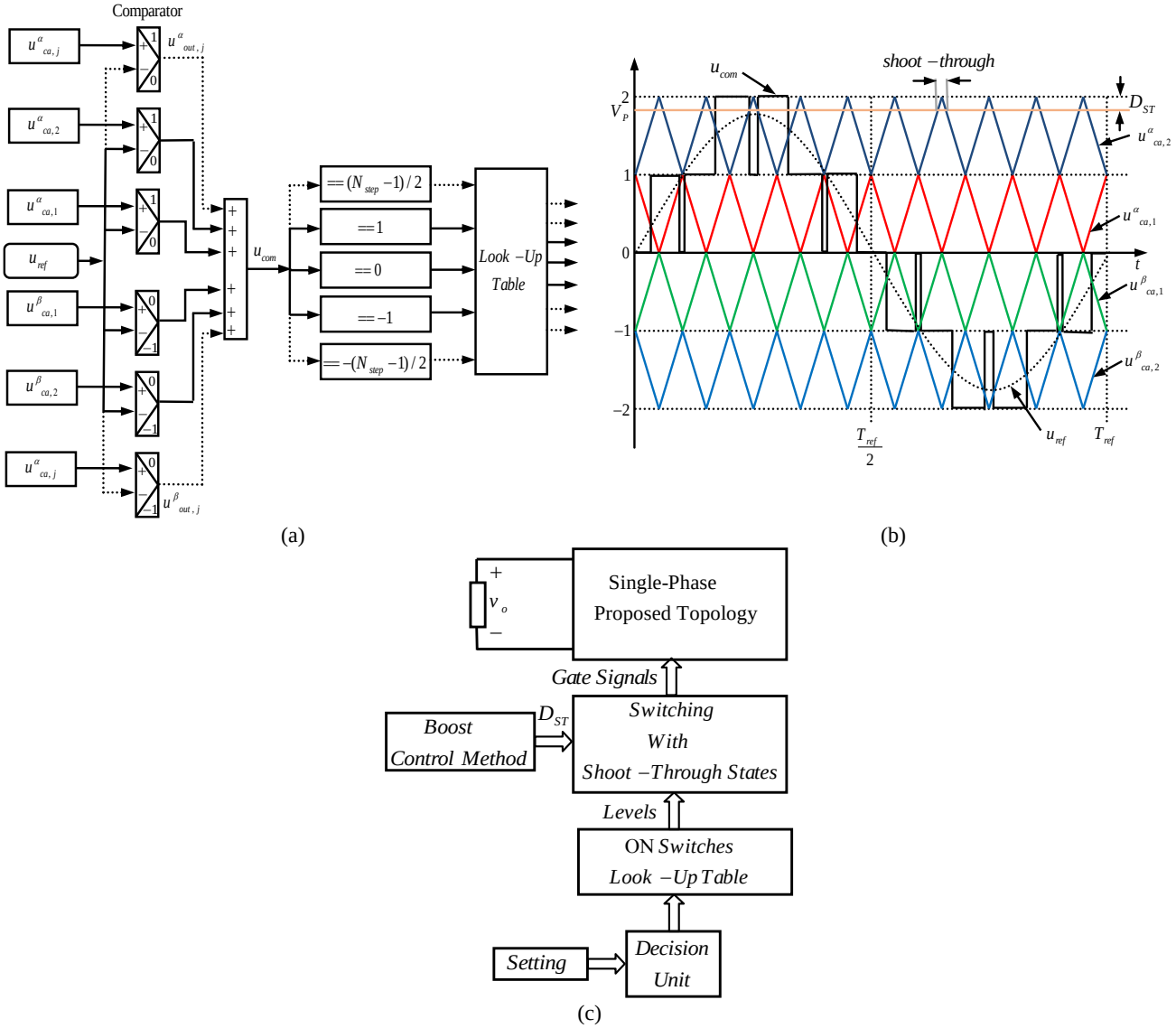

Fig. 5 Proposed topology control method; a) Control method scheme, b) Waveforms pertaining to the control scheme for 5-level, and c) Control block diagram.

Triangular carrier waves above the axis are indicated with $u_{ca,j}^{\alpha}$ and below the axis are indicated with $u_{ca,j}^{\beta}$, ($j = 1, 2, \ldots, \frac{N_{step}-1}{2}$).

If the reference signal (u_{ref}) is greater than the triangular carrier wave above the axis ($u_{ca,j}^{\alpha}$), the comparator output is 1, otherwise is 0. If reference signal (u_{ref}) is greater than the triangular carrier wave below the axis ($u_{ca,j}^{\beta}$), the comparator output is 0, otherwise is -1, which is as follows:

$$u^{\alpha}{}_{out,j} = \begin{cases} 1 & \text{if } u_{ref} \geq u^{\alpha}{}_{ca,j} \\ 0 & \text{otherwise} \end{cases} \quad (55)$$

$$u^{\beta}{}_{out,j} = \begin{cases} 0 & \text{if } u_{ref} \geq u^{\beta}{}_{ca,j} \\ -1 & \text{otherwise} \end{cases} \quad (56)$$

In above relations, $u_{ca,j}^{\alpha}$ and $u_{ca,j}^{\beta}$ are comparators output for carrier waves above the axis and below the axis, respectively.

Obtained results from (55) and (7) are added as:

$$u_{com} = \sum_{j=1}^{\frac{N_{step}-1}{2}} \left(u^{\alpha}{}_{out,j} + u^{\beta}{}_{out,j} \right) \quad (57)$$

In above relation, u_{com} is the composite signal. Switching signals for each power electronic switches can be obtained by u_{com} and logical circuits according to converter look-up table.

In order to establish ST state for quasi-Z-source converter, the simple boost control method is used [36-37]. The main control idea for quasi-Z-source converter is the conversion of conventional zero states to ST state without changing active switching states. For instance for establishing ST state for first quasi-Z-source converter in the first basic unit (QZS_{11}), when the switch S'_{11} is on, the switch S_{11} for ST duty cycle duration (T_{ST}) is being on, so that ST state can be provided for the converter. In this method, one straight line (V_P) is used to control ST state time interval. If the magnitude of the upper carrier signal of $u^{\alpha}{}_{ca}$ is greater than the magnitude of V_P ($u^{\alpha}{}_{ca} > V_P$) then basic unit is in the ST state.

Due to this fact that for each quasi-Z-source network can control value of duty ratio; so, control system of each network should adjust its DC output voltage in the desired value. This issue can be done by using close loop control of output voltage. In close loop control, at any moment (due to sample time) feedback is taken from output voltage and at any moment value of duty cycle is updated and this issue brings output voltage of converter to value of reference voltage. The failure to control can lead to improper output voltage and impaired performance of proposed topology.

6 Comparison

In the multilevel inverters, rating of power switches is one of the most important challenges. Total cost of implementation of a multilevel inverter is directly related to rating of voltage and current of power switches [38]. In the proposed topology, rating of current of each switch depends on current of load and is considered equal to it. Hence due to load of proposed topology, current of load should be calculated and appropriate switch should be selected. In the references and literatures, two concepts about rating of voltage are discussed. The first concept is peak inverse voltage (PIV) and the second concept is standing voltage (SV). In the proposed topology, PIV for all switches is obtained as follows:

$$PIV = \sum_{j=1} V_{switch,j} \quad (58)$$

where $V_{switch,j}$ is peak inverse voltage of the j-th switch.

In the proposed topology, total PIV for each three proposed strategies is calculated as follows:

$$PIV = V_{dc} \left(N_{step} - 1 \right) \quad (59)$$

According to [15], the above-mentioned equation can be considered as maximum standing voltage of switches. In the proposed topology, total standing voltage (TSV) is calculated as follows:

$$TSV = PIV_S + PIV_T \quad (60)$$

where PIV_S is related to PIV of available switches in the units and PIV_T is related to PIV of available switches in the full-bridge segment.

By substituting (59) in (60), TSV of proposed topology is obtained as follows:

$$TSV = 2V_{dc} \left(N_{step} - 1 \right) \qquad N_{step} \geq 2 \quad (61)$$

The per-unit value of TSV is defined as follows:

$$TSV_{pu} = \frac{TSV}{V_{dc}} = 2\left(N_{step} - 1 \right) \qquad N_{step} \geq 2 \quad (62)$$

Fig. 6 shows comparison of TSV between proposed topology and presented multilevel inverters in [14-15]. According to this figure, the value of TSV for the proposed topology is not higher than TSV of presented topologies in [14-15].

Fig. 7 shows comparison of number of used switches in the proposed topology with three proposed strategies and presented topologies in [14-15]. According to this figure, to have same voltage level, number of switches for the proposed topology in each three strategies is lower; so, gate driver circuits and power losses will be

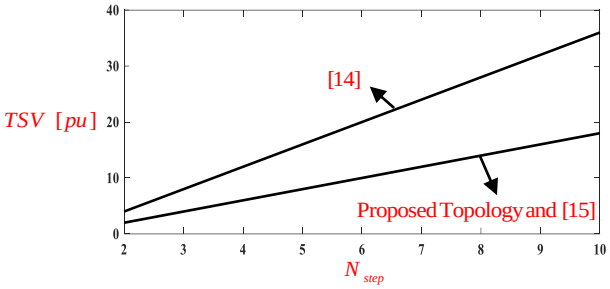

Fig. 6 Comparison of TSV.

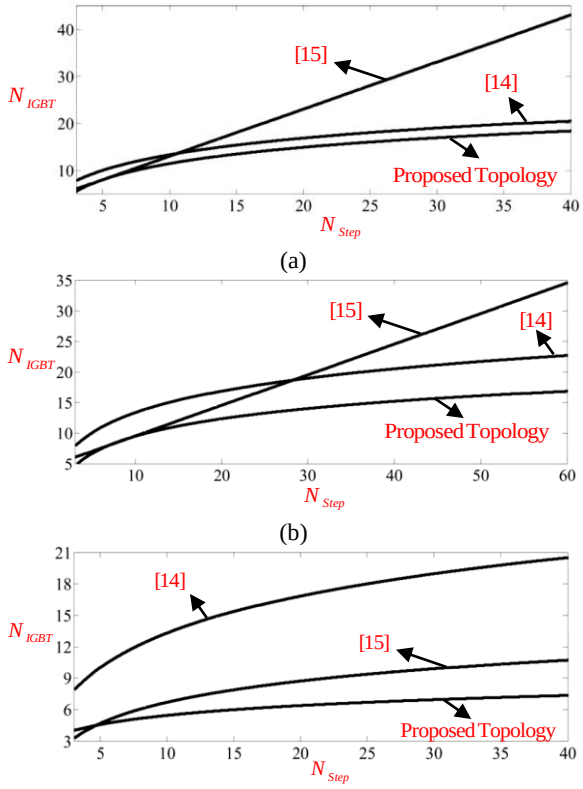

Fig. 7 Comparison of number of switches versus number of levels; a) The first strategy, b) The second strategy, and c) The third strategy.

low.

Although the proposed multilevel inverter based on quasi-Z-source does not have lower number of passive elements in comparison with conventional multilevel inverters but number of elements in the proposed topology is lower in comparison with conventional Z-source multilevel inverter which has application in photovoltaic systems. In the mentioned application, photovoltaic cells are used instead of DC power supplies and use of DC/DC converter is necessary for increasing the voltage gain and obtaining maximum power. In the proposed topology, quasi-Z-source network is used instead of DC/DC converter which has no power switch and transferring the power is done only in one stage. As a result, it is necessary to use a converter for photovoltaic applications and due to lack of power switch in the quasi-Z-source network, high number of passive elements in the proposed topology is justifiable.

7 Simulation Results

To investigate operation of proposed multilevel converter based on quasi impedance-source network, simulation results using PSCAD/EMTDC software for single phase topology with 25 levels are provided. Power circuit of this topology is shown in Fig. 8. In this figure for determining DC voltage sources, the first proposed strategy is used [39].

The proposed topology is designed for generating 25 levels with frequency of $50Hz$. In the simulation, output load is resistive/inductive with values of $R = 107\ \Omega$ and $L = 55$ mH. Values of other parameters in the simulation are presented in Table 3. In Table 4, switching states of inverter are shown for producing different voltage levels. The inverter is able for generating all odd and even voltage levels.

By using presented values in Table 3 and (14), maximum value of voltage in the output of both quasi-Z-networks in the first basic cell is 10 V. Moreover, maximum value of voltage in the output of both quasi-Z-networks in the second basic cell is 50 V. Figs. 9(a) and 9(b) show waveforms of output voltage in the quasi-impedance networks for both basic cells. According to these figures, output voltage of quasi-Z-networks in the ST state is zero and in the non-ST state is non-zero. Figs. 9(c) and 9(d) show maximum output voltage of quasi-Z-source converter in the first and second basic cell, respectively. According to these figures, maximum output voltages of quasi-Z-source converter in the first and second cells are 10 V and 50 V, respectively.

Fig. 10 shows simulation results for proposed multilevel inverter. According to this figure, output voltage of each basic unit (v_1 & v_2) always has a zero or positive value. Output ac voltage of full-bridge inverter (v_{o1} & v_{o2}) are in series with each other and combined output voltage (v_o) is sum of the output voltages of full-bridge converters. As shown in Fig. 10, output voltage is a sinusoidal voltage with frequency of 50 Hz which has 25 levels from -120 V to +120 V. It is noticeable that there is a phase difference between waveforms of output voltage and output current. The reason of this subject is inductive characteristic of output load. Moreover, output voltage has sinusoidal waveform with low value of total harmonic distortion [40].

8 Experimental Results

In this section, the experimental results of proposed basic unit structure composed of two voltage sources and two quasi-Z-source converters (Fig. 11) are presented. The first proposed algorithm is employed to determine the magnitude of DC voltage sources. The parameters of base unit are illustrated in Table 5. In

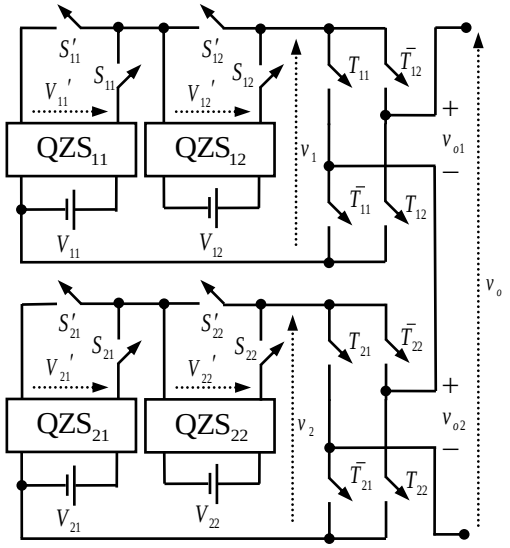

Fig. 8 Used topology in simulation for generating 25 levels.

Table 3 The values of parameters in the simulation.

Parameters	Values
$L_1 = L_2$	5 mH
$C_1 = C_2$	600 µF
f_{ref}	50 Hz
f_s	20 kHz
D_{ST}	0.1
$V_{11} = V_{12}$	8 V
$V_{21} = V_{22}$	40 V

Table 4 Switching states of converter for generating different voltage levels.

v_o [pu]	Switching States							
	S_{11}	S_{12}	S_{21}	S_{22}	T_{11}	T_{12}	T_{21}	T_{22}
-12	1	1	1	1	1	1	1	1
-11	0	1	1	1	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
-1	1	0	0	0	1	1	1	1
0	0	0	0	0	1	1	1	1
1	1	0	0	0	0	0	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
11	0	1	1	1	0	0	0	0
12	1	1	1	1	0	0	0	0

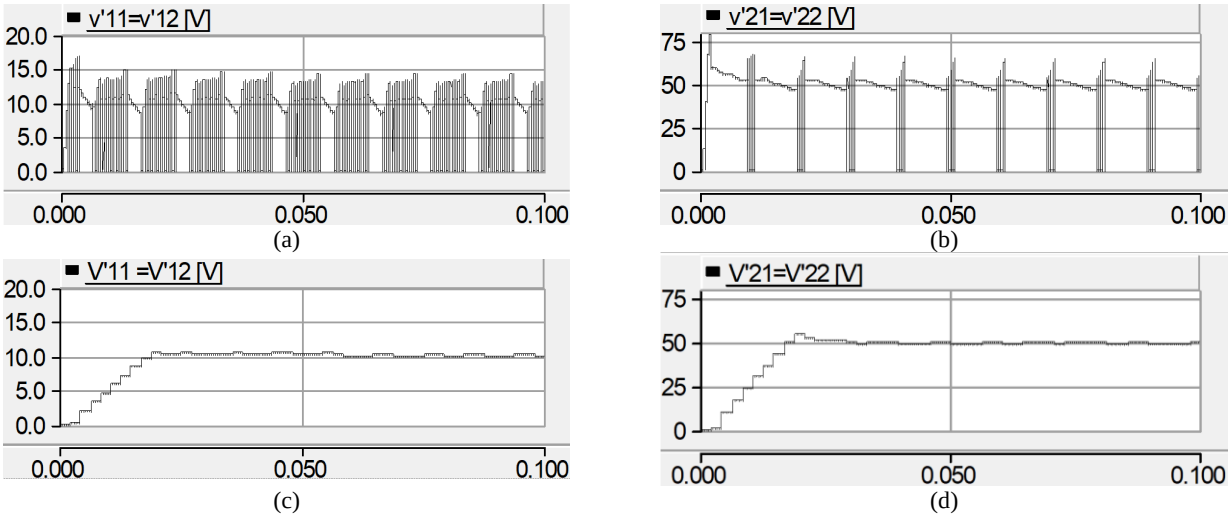

Fig. 9 Output voltage waveform of quasi-Z-source network; a) Output voltage waveform of quasi-Z-source network in the first basic cell, (b) Output voltage waveform of quasi-Z-source network in the second basic cell, c) Maximum output voltage waveform of quasi-Z-source network in the first basic cell, and d) Maximum output voltage waveform of quasi-Z-source network in the second basic cell.

order to produce 5 levels at the output voltage, the explained control method is used. To establish ST state for quasi-Z-source converter, the simple boost control method is used.

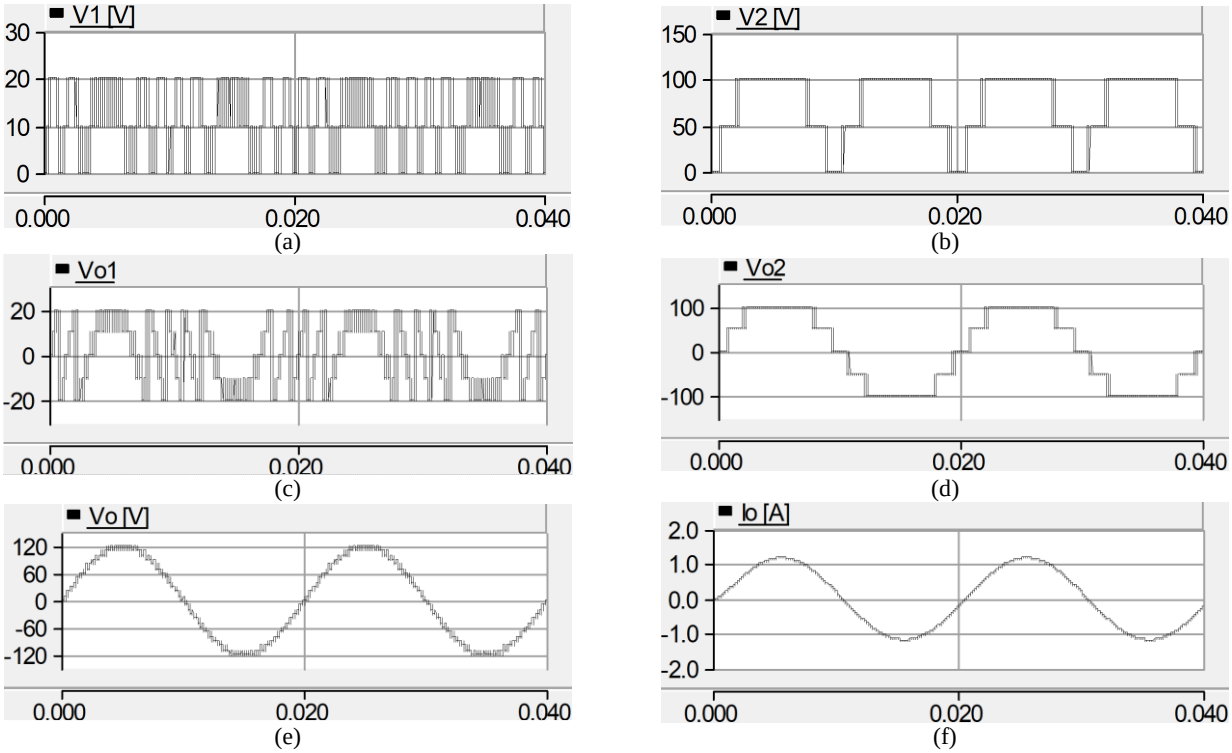

Fig. 10 Simulation results of proposed topology; a) Output voltage waveform of the first basic unit, b) Output voltage waveform of the second basic cell, c) Output voltage waveform of the first multilevel inverter, d) Output voltage waveform of the second multilevel inverter, e) Output voltage of proposed topology, and f) Output current of proposed topology.

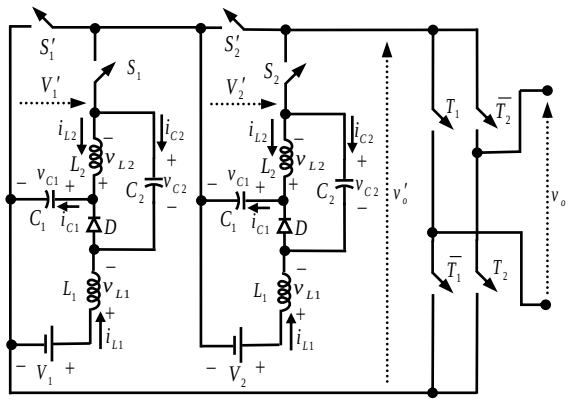

Fig. 11 Implemented 5-level inverter.

The duty cycle of ST for quasi-Z-source converter is assumed as D_{ST} = 0.25 and the value of each DC voltage sources are 50 V. Then according to (14), the maximum voltage at the output of each quasi-Z-source converter will be 100 V.

Figs. 12(a) and 12(b) show output voltage waveforms of both quasi-Z-source converters. As can be seen from these figures, the output voltages of both quasi-Z-source converters are equal and the maximum values of them are approximately 100 V. It can be observed that DC-link voltage in ST state is zero and in the non-ST state is equal to 100 V. Fig. 12(c) shows output voltage of cascaded structure (v_o') for three-level voltage. The waveform of full-bridge output voltage or load voltage (v_o) for five-level voltage is shown in Fig. 12(d). The load voltage and current are shown in Fig. 12(e). The phase difference between the load voltage and current is due to inductive characteristic of load. The small difference between the experimental and theoretical results is due to the non-ideal of components.

Table 5 The values of parameters in the experimental prototype.

Parameters	$L_1 = L_2$	$C_1 = C_2$	f_{ref}	f_s	D_{ST}	$V_1 = V_2$	R_{Load}	L_{Load}
Values	2 mH	680 μF	50 Hz	10 kHz	0.25	50 V	107 Ω	55 mH

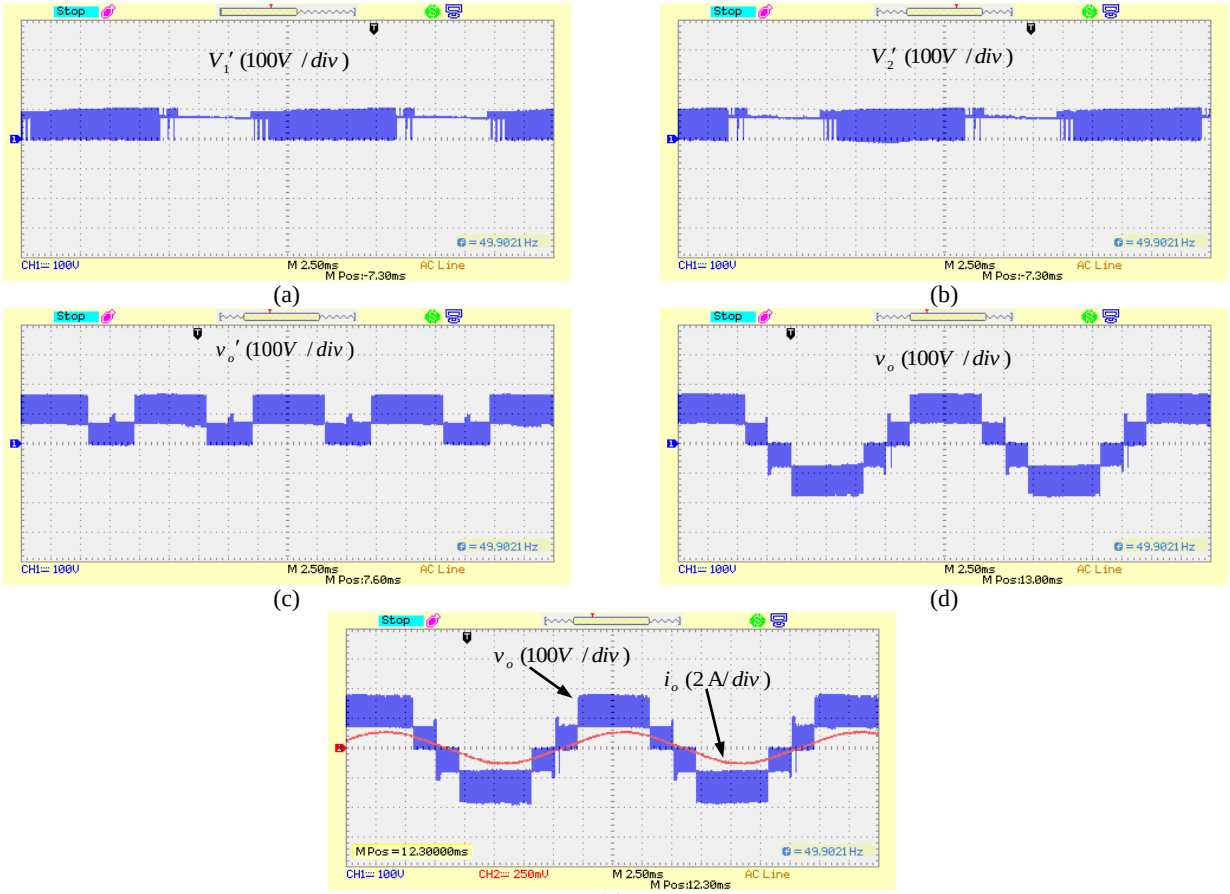

Fig. 12 Experimental results; a) DC-link voltage of first quasi-Z-source converter (V_1'); (b) DC-link voltage of second quasi-Z-source converter (V_2'); (c) DC-link voltage of quasi Z-source converter in a small interval; (d) v_o'; (e) v_o; (f) Load voltage and current (v_o and i_o).

9 Conclusion

In this paper, a new topology for cascaded multilevel inverter based on quasi-Z-source converter was proposed. Due to the use of quasi-Z-source converter in the proposed topology, the magnitude of DC voltage sources can be increased. As a result, no additional DC-DC converter was needed. In the proposed topology, the magnitude of DC voltage sources can be increased by increasing of ST duty cycle of quasi-Z-source converter. As an example, for $D_{ST} = 0.25$, voltage gain of the proposed topology was 2. In this paper, the quasi-Z-source structure in two operation modes of ST and non-ST, was analyzed and the equations of the voltages across inductors, capacitors and gain voltage was calculated. Also, the values of components in quasi-Z-source network were designed. In proposed topology, due to short circuit capability and increased DC voltage source magnitude by quasi-Z-source converter, the reliability of proposed topology is increased and the output voltage is not limited to the DC voltage source.

To provide a large number of output steps without increasing the number of inverters, asymmetric structures was used and three algorithms to determine the magnitude of DC voltage sources was proposed. The proposed topology has been optimized for various purposes of obtaining minimum switch numbers and DC voltage sources, and maximum numbers of voltage level. Also, to provide output steps and ST state for quasi-Z-source converter, proposed control method was explained. The operation and performance of the proposed topology has been verified with simulation and experimental results. It was shown that the proposed topology has a good performance.

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