

A Novel Active Feedback Frequency Compensation Scheme for Two-Stage OTA

H. Faraji Baghtash^{*(C.A.)} and Kh. Monfaredi^{**}

Abstract: A novel active feedback frequency compensation scheme is presented in this work. Based on the proposed technique, an amplifier with two main poles in its frequency bandwidth can be easily compensated by introducing a pole-zero pair in a local feedback. The proposed method is mathematically analyzed and then based on the derived formulations, a design procedure is established. The capability of the proposed technique is examined considering a well-known two-stage amplifier, considering just a trivial modification on its input stage. To gain an analogous and fair insight, the performance of the proposed structure is compared with that is of the optimally designed miller-compensated two-stage amplifier. The post-layout simulations are accomplished with TSMC 180nm CMOS standard technology. The Spectre post-layout simulations show that the proposed structure outperforms the traditional structure in terms of power consumption and gain bandwidth product. The robustness of the design is checked with Monte Carlo simulations.

Keywords: Low Voltage, Low Power, Frequency Compensation, Operational Amplifier.

1 Introduction

OPERATIONAL trans-conductance amplifier (OTA), is essentially one of the most common and widely used blocks in analog signal processing [1-4]. Beside its vast usage in application requiring signal amplification, they have been also known as versatile blocks, finding widespread applications in many structures such as voltage followers, current-to-voltage convertors, active rectifiers, integrators, and various types of filters. Among other specifications of the OTA blocks, the DC-gain and operating frequency bandwidth are considered as the two most important parameters that normally required to be maximized during the design procedure. Unfortunately, there is a severe tradeoff between these two parameters, which means that improving one of these parameters will strictly

degrade the other one. Cascoding and cascading of the amplifier blocks are two most common approaches for boosting the overall gain. Due to the supply voltage scaling imposed by nowadays technology downscaling, the performance improvement expected by cascoding is essentially diminished, while the cascading gains more attention than ever. Unfortunately, cascading degrades the stability of the overall amplifier. Hence, the two cascaded stages are typically preferred to maintain the desirable stability. Even with two cascaded stages, the overall amplifier is usually prone to be unstable when used in feedback configurations. Hence the frequency compensation is usually required for two stage OTAs.

So far, several frequency compensation techniques have been proposed for two-stage amplifiers, all of which are variants of well-known Miller compensation scheme [5]. In this scheme, a Miller capacitance is usually inserted between input and output nodes of the second stage (gain stage) [6-9]. This moves the poles of amplifier in opposite directions along the frequency axis, and hence by decreasing the frequency of dominant pole and increasing the frequency of non-dominant pole, improves the amplifier stability. The pure Miller compensation technique, however, produces a right half-plane zero. Different variants of Miller compensation scheme have somehow tried to either

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* The author is with the Faculty of Electrical Engineering, Sahand University of Technology, Tabriz, Iran.

E-mail: hfaraji@sut.ac.ir.

** The author is with the Faculty of Engineering, Azarbaijan Shahid Madani University, Tabriz, Iran.

E-mail: khmonfaredi@azaruniv.ac.ir.

Corresponding Author: H. Faraji Baghtash.

eliminate this right half-plane zero or to turn it to a left half-plane one. For instance, a nulling resistor added in series with the compensation capacitor, makes it possible to effectively remove the right half-plane zero or turn it to a left half-plane zero [10, 11]. Some other variants of Miller compensation have been proposed which exploit voltage follower [12-14], current follower [12, 13, 15, 16], current amplifier [15], or current mirror [17, 18] in feedback or feedforward path.

The miller scheme is indeed proved to be a very effective compensation technique. Although the theory and design procedure of the miller compensation technique are well-established, and hence can be easily used to compensate any two-stage amplifier, but, it has some disadvantages as well. For instance, the miller capacitor degrades the slew rate and destroys the PSRR of the amplifier.

In this work a novel active feedback frequency compensation scheme is presented for two-stage OTAs. The proposed scheme is an alternative method to the conventional miller compensation technique, which effectively overcomes its PSRR degradation problem. The proposed approach requires a much smaller capacitor; leading to a less occupied chip area and adds no extra power to the original amplifier.

The paper is organized as follows. Section 2 describes the concept of the proposed technique. The principal of operation and related mathematical formulations are provided in this section. The simulation results are given in Section 3 and finally, section 4 concludes the paper.

2 The Proposed Compensation Scheme

An appropriately designed two-stage uncompensated amplifier normally has two separate poles with no zeros in its frequency bandwidth. Therefore, the simplified s-domain frequency transfer function of a two-stage amplifier can be given by:

$$A(s) = \frac{A_0}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} = \frac{A_0 p_1 p_2}{(p_1 + s)(p_2 + s)} \quad (1)$$

where, A_0 , p_1 , and p_2 are DC gain, first, and second poles of the amplifier, respectively. Since the amplifier is not frequency compensated, both p_1 and p_2 are smaller than unity-gain bandwidth (GBW), i.e. $p_1 < p_2 < \text{GBW}$.

To explain the frequency compensation scheme, let us put the amplifier, $A(s)$, in a feedback loop, as in Fig. 1, and derive some formulas. Doing so, the frequency compensation scheme will be discussed and its effectiveness will be verified as we proceed.

Fig. 1 shows the block diagram of a negative feedback amplifier which is formed by an amplifier "A" and a feedback block " β ". The closed-loop transfer function of this feedback system (like that in Fig. 1) is clearly given

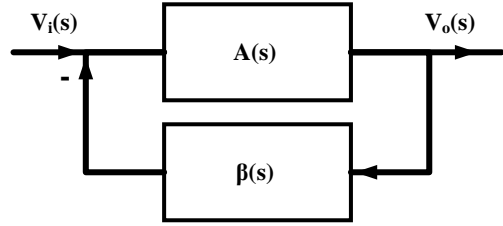


Fig. 1 Amplifier "A" in a feedback loop.

by:

$$\frac{V_o}{V_i}(s) = A_{CL}(s) = \frac{A(s)}{1 + A(s)\beta(s)} \quad (2)$$

The main idea here is to choose the transfer function of $\beta(s)$ such that the $A_{CL}(s)$ be frequency compensated. To do so, suppose that $\beta(s)$ is given by:

$$\beta(s) = \frac{\beta_0 s}{p_f + s} \quad (3)$$

where, p_f is the pole frequency of $\beta(s)$ and β_0 is a constant coefficient. Substituting $A(s)$ and $\beta(s)$ from (1) and (3) into (2) gives:

$$A_{CL}(s) = \frac{A_0 p_1 p_2 (p_f + s)}{p_1 p_2 p_f + \lambda s + (p_1 + p_2 + p_f)s^2 + s^3}, \quad (4)$$

$$\lambda = p_1 p_2 + p_1 p_f + p_2 p_f + A_0 \beta_0 p_1 p_2$$

Assuming that $p_1 < p_2 < p_f < A_0 \beta_0 p_1$, Eq. (4) can be simplified to:

$$A_{CL}(s) = \frac{A_0 p_1 p_2 (p_f + s)}{\left(\frac{p_1 p_f}{p_f + A_0 \beta_0 p_1} + s\right) D(s)}, \quad (5)$$

$$D(s) = (p_f + A_0 \beta_0 p_1) p_2 + p_f s + s^2$$

Examining (5) reveals that the only condition in which $A_{CL}(s)$ may offer a favorable phase margin (PM) is when $D(s)$ has a $\Delta < 0$, i.e. two complex roots. Now, let us evaluate a condition in which the proper phase margin can be achieved. To do so, one may proceed as follows: If we define $\alpha = p_1 A_0 / p_f$, Eq. (5) can be rewritten as:

$$A_{CL}(s) = \frac{A_0 p_1 p_2 \left(\frac{p_1 A_0}{\alpha} + s\right)}{\left(\frac{p_1}{1 + \alpha \beta_0} + s\right) D(s)}, \quad (6)$$

$$D(s) = A_0 \frac{(1 + \alpha \beta_0)}{\alpha} p_1 p_2 + \frac{p_1 A_0}{\alpha} s + s^2$$

At unity-gain bandwidth frequency of $\omega_0 = p_1 A_0 / (1 + \alpha \beta_0)$, the amplitude of the closed-loop transfer function should be unity, i.e. $|A_{CL}(\omega_0)| = 1$.

Considering this condition gives:

$$\left[\frac{1 + \alpha\beta_0}{\alpha} - \frac{p_1 A_0}{p_2} \cdot \frac{1}{(1 + \alpha\beta_0)^2} \right]^2 + \left[\frac{p_1}{p_2} \cdot \frac{A_0}{\alpha(1 + \alpha\beta_0)} \right]^2 - \left(\frac{1 + \alpha\beta_0}{\alpha} \right)^2 = 1 \quad (7)$$

On the other hand, at unity-gain bandwidth frequency, the phase margin requirement should be satisfied as well, i.e. $PM = \angle A_{CL}(\omega_0) + 180$. Calculating the PM of (6) at $\omega = \omega_0$ gives:

$$PM = 180 + \tan^{-1}\left(\frac{\omega_0}{p_f}\right) - \tan^{-1}\left(\frac{\omega_0(1 + \alpha\beta_0)}{p_1}\right) - \angle D(s),$$

$$\angle D(s) = \tan^{-1}\left(\frac{\alpha(2\omega_0 - \sqrt{|\Delta|})}{p_1 A_0}\right) + \tan^{-1}\left(\frac{\alpha(2\omega_0 + \sqrt{|\Delta|})}{p_1 A_0}\right) \quad (8)$$

where, Δ is given by:

$$\Delta = \left(\frac{p_1 A_0}{\alpha}\right)^2 - 4A_0 \frac{(1 + \alpha\beta_0)}{\alpha} p_1 p_2 \quad (9)$$

Replacing ω_0 by its equivalence in (8) gives:

$$PM = 90 + \tan^{-1}\left(\frac{\alpha}{1 + \alpha\beta_0}\right) - \angle D(s),$$

$$\angle D(s) = \tan^{-1}\left(\left[\frac{2\alpha}{1 + \alpha\beta_0} - \sqrt{\frac{4p_2\alpha(1 + \alpha\beta_0)}{p_1 A_0} - 1}\right]\right)$$

$$+ \tan^{-1}\left(\left[\frac{2\alpha}{1 + \alpha\beta_0} + \sqrt{\frac{4p_2\alpha(1 + \alpha\beta_0)}{p_1 A_0} - 1}\right]\right) \quad (10)$$

Solving (7) and (10), gives the values of α and β_0 that satisfy the required phase margin. The resulted values are not exact, as some approximations have been considered to derive these equations; however, they give a good start point to initiate some iterations to find the proper values that truly satisfy the phase margin requirements.

In the following section the realization of the proposed compensation scheme on a two stage amplifier is discussed.

3 Circuit Realization Based on the Proposed Scheme

In this section, the proposed compensation method is embedded on a well-known two stage amplifier to examine its performance. Let us initially investigate the effect of the proposed scheme on an ideal two-pole op-amp block, before considering the aforementioned two stage amplifier. Fig. 2(a) depicts a realization of the

proposed compensation technique where, $\beta(s)$ is given by $\beta(s) = s/(s + 1/RC)$. As can be seen in Fig. 2(a), despite the simple realization of the proposed technique, this configuration imposes a serious limitation on the compensated amplifier. In other words, its negative input is not available anymore when it is utilized in a feedback loop. To resolve this issue, the amplifier structure requires a little modification. This can be simply accomplished by adding an extra inverting input to the amplifier considering, as is shown in Fig. 2(b). Considering this inverting input, the amplifier has two distinct inverting ports, one is used for the realization of the compensation network and the other one is available for any other application, such as general feedback network configuration. Undoubtedly, this is not the only application that the proposed scheme can be applied to, and other configurations compatible with the proposed compensation technique can be certainly found or developed. Nevertheless, this article aims to show the performance of the proposed compensation scheme in a simple configuration.

Fortunately, the realization of the modified 3-input amplifier is very straightforward. Fig. 3 depicts the transistor level implementation of the modified amplifier. As it can be seen in Fig. 3, the third input is obtained simply by embedding an extra NMOS transistor satisfying the DMOS design methodology conditions [19], highlighted with red color, in the differential pair of amplifier.

Now, let us derive some formulations for expressing some of the small-signal characteristics of the proposed amplifier shown in Fig. 3.

3.1 The Frequency Response Analysis

Considering the resistances seen from the drains of Mp2 and Mp3, respectively as R_I and R_{II} , and regarding that $g_{m1} = g_{m2} = g_{m3} = g_I$ and $g_{mp3} = g_{II}$, the following equations can be written.

$$V_{out} = -g_{II} R_{II} \left(-g_I V_{gs2} + \frac{g_I V_{gs1}}{2} + \frac{g_I V_{gs3}}{2} \right) R_I \quad (11)$$

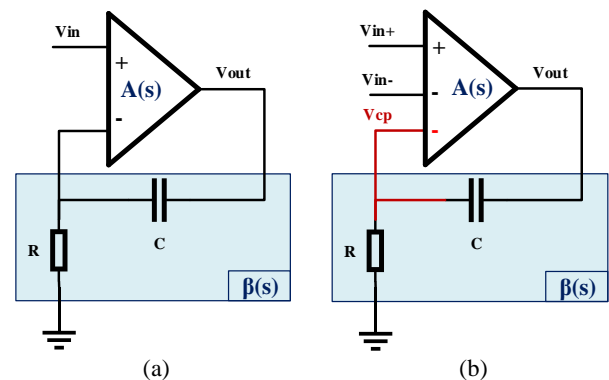


Fig. 2 Realization of the proposed compensation scheme on an ideal two-pole Amplifier, a) the original, and b) the modified version.

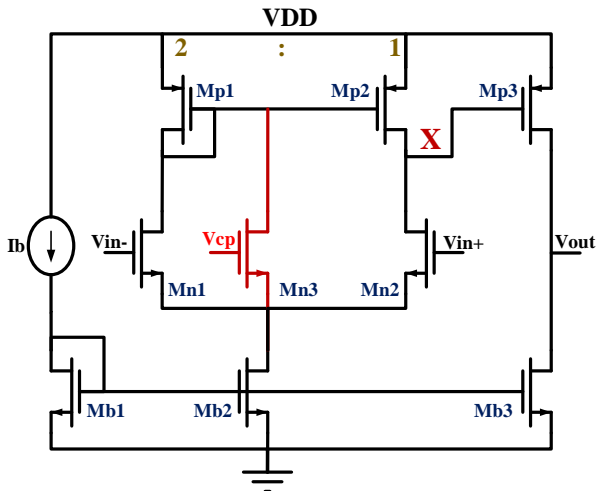


Fig. 3 The transistor level realization of the 3-input amplifier.

where,

$$R_I = r_{op2} + 1.5r_{on2}, \quad R_{II} = r_{op3} + r_{ob3} \quad (12)$$

Performing some simplifications gives:

$$V_{out} = g_I g_{II} R_I R_{II} \left(V_{in+} - \frac{V_{in-}}{2} - \frac{V_{cp}}{2} \right) \quad (13)$$

From (12), it can be observed that if the two negative input ports of the proposed amplifier are tied together, the proposed amplifier acts as a regular amplifier (with two input ports) with differential DC gain of $A_V(0) = g_I g_{II} R_I R_{II}$. On the other hand, if the proposed amplifier is configured as Fig. 2(b) with positive input node tied to the ground ($V_{in+} = 0$), the DC voltage gain is given by $A_V(0) = g_I g_{II} R_I R_{II} / 2$.

Considering $V_{in+} = 0$ and substituting $V_{cp} = \beta V_{out}$ into (13) gives:

$$\frac{V_{out}}{V_{in-}} = -\frac{A_0}{1 + A_0 \beta} \quad (14)$$

where,

$$A_0 = \frac{g_I g_{II} R_I R_{II}}{2} \quad (15)$$

So far, the effects of the parasitic capacitances are neglected in gain analysis, yielding just the DC voltage gain. As it will be shown in the next section (see Fig. 4), the proposed amplifier has two distinct poles in its operating frequency range. Considering Fig. 3, these two poles occur at frequencies equal to $p_1 = 1/R_I C_I$ and $p_2 = 1/R_{II} C_{II}$, where, C_I and C_{II} are given by (16), Hence, Eq. (14) can be rewritten as (17)

$$C_I = c_{dsp2} + c_{dsn2} + c_{gsp3}, \quad (16)$$

$$C_{II} = c_{dsp3} + c_{dsb3} + c_L$$

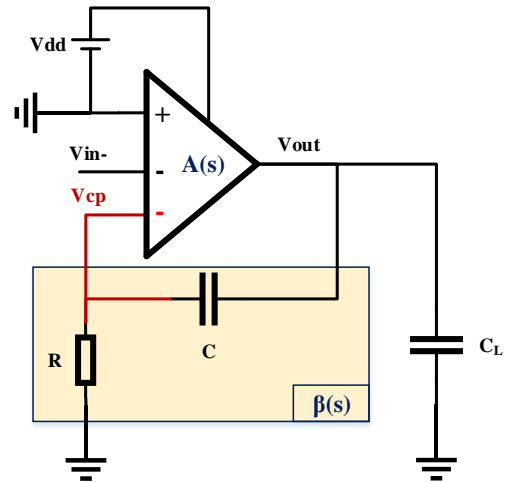


Fig. 4 The configuration of the proposed amplifier to evaluate the PSRR.

$$\frac{V_{out}}{V_{in-}} = -\frac{A(s)}{1 + A(s)\beta(s)}, \quad \beta(s) = \frac{RCs}{1 + RCs},$$

$$A(s) = \frac{A_0}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \quad (17)$$

The Eq. (17) shows that if the proposed amplifier is configured as Fig. 2(b), its frequency transfer function is Analogous with that is of Fig. 1 (refer to (2)). Therefore, the formulations derived in previous section can be exploited to obtain the frequency response of the compensated amplifier, as well as, the corresponding values for R and C that satisfy (10).

3.2 The PSRR Analysis

To evaluate the PSRR of the proposed circuit, consider the amplifier configuration as in Fig. 4, where the power supply variations is shown with V_{dd} . Respecting this figure, the output voltage can be defined as:

$$V_{out} = -\frac{A(s)}{2} V_{in-} - \frac{A(s)}{2} V_{cp} + A_{dd}(s) V_{dd} \quad (18)$$

where $A_{dd}(s)$ is the voltage gain from V_{dd} to V_{out} . Replacing V_{cp} with βV_{out} in (18) gives:

$$V_{out} = -\frac{A(s)}{2 + A(s)\beta(s)} V_{in-} + \frac{2A_{dd}(s)}{2 + A(s)\beta(s)} V_{dd} \quad (19)$$

Recalling the definition of the PSRR which is given by $(V_{out}/V_{in})/(V_{out}/V_{dd})$, from (19), the PSRR of the proposed circuit is given by:

$$|PSRR| = \frac{A(s)}{2A_{dd}(s)} \quad (20)$$

The $A(s)$ already is defined in (17), though if $A_{dd}(s)$ can be determined properly, the PSRR can be obtained accordingly. To do so, we need to tie the inputs of the amplifier to the ground and obtain the transfer function from V_{dd} to V_{out} . Fortunately, in this configuration, the proposed amplifier acts exactly like a traditional uncompensated two-stage amplifier. Therefore, $A_{dd}(s)$ is given by [20, 21]:

$$A_{dd}(s) \approx \frac{1}{1 + \frac{s}{p_1}} \tag{21}$$

Substituting $A(s)$ and $A_{dd}(s)$ from (17) and (21) in to (20) gives the PSRR value as:

$$|PSRR| = \frac{A_0}{2 \left(1 + \frac{s}{p_2} \right)} \tag{22}$$

4 Post-Layout Simulation Results

The performance of the proposed compensation

scheme and its application on the modified two-stage amplifier (see Fig. 3) is investigated through Spectre post-layout simulations with TSMC 180nm CMOS standard technology. After compensation, the performance of the proposed structure is compared with that is of the traditional two-stage miller-compensated amplifier. To have a fair comparison, each amplifier is optimally designed and compensated to have 50° phase margin at the presence of a 30pF load capacitance. The layout view of the amplifiers is shown in Fig. 5. The transistors’ aspect ratios and the amplifiers’ bias conditions are summarized in Table 1.

The frequency behavior of an uncompensated two-stage amplifier, with the specifications given in Table1, is shown in Fig. 6. This figure shows that the amplifier has two poles in its frequency bandwidth, making the frequency compensation necessary to enable the amplifier to be appropriately used in feedback configurations. The poles are evaluated to be $p_1 = 162$ kHz and $p_2 = 18.75$ MHz.

Table 1 The bias conditions and transistors’ dimensions.

Device Name	Traditional	Proposed
Ib	56 μA	100 μA
Mb1	27μm/540nm	27μm/540nm
Mb2	108μm/540nm	108μm/540nm
Mb3	540μm/540nm	54μm/540nm
Mn1, Mn2	56μm/180nm	56μm/180nm
Mn3	NA	56μm/180nm
Mp1	140μm/540nm	280μm/540nm
Mp2	140μm/540nm	140μm/540nm
Mp3	2*700μm/540nm	140μm/540nm

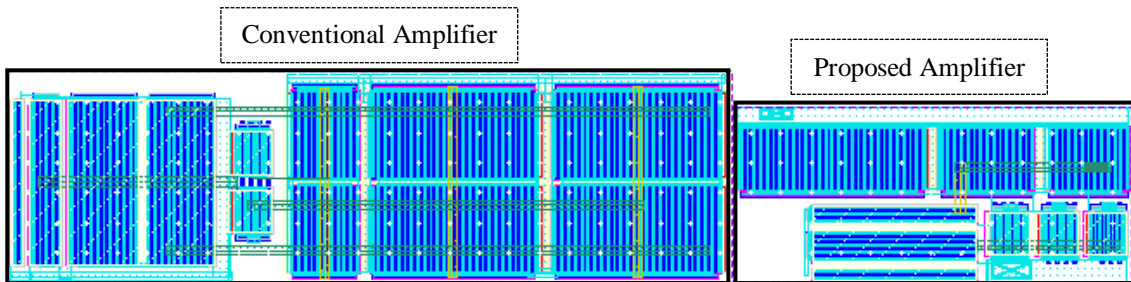


Fig. 5 The layout view of the design.

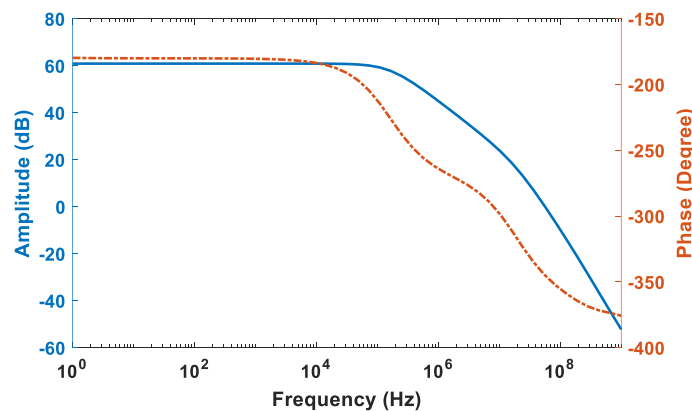


Fig. 6 The frequency behavior of the uncompensated two-stage amplifier.

The numerical values of α and β_0 must be obtained to compensate the circuit with the proposed compensation scheme. Considering the configuration of Fig. 2(b), the value of β_0 is obtained 0.66. Substituting the values of β_0 , p_1 , and p_2 into (10), gives the value of α for a specified PM. Taking 50° phase margin into account, the value of α evaluated to be 2.23. The value of α equal with 2.23 is translated to the 80MHz pole frequency in the feedback network, i.e. $p_f = 80MHz$. This gives the RC value of about 2ns. Selecting the value of $R = 6k\Omega$, gives the value of $C = 0.33pF$. Simulating the compensated amplifier with the values obtained for R and C, the phase margin of about 47° is obtained which is very close to the desired value. To achieve a strictly precise result, the design is re-simulated by sweeping the value of C around its predicted value. This gives the proper value for C, that is $C = 0.4pF$, which essentially delivers the required 50° phase margin. As stated in the first paragraph of this section, an optimally designed miller compensated amplifier is considered to compare its performance with that is of the proposed structure. Fig. 7 shows the frequency behavior of the proposed circuit versus frequency behavior of the traditional miller compensated amplifier.

As can be observed from Fig. 7, both of the amplifiers deliver the same amount of PM, which is about 50° . Comparing the results, it is clear that the traditional amplifier presents a little higher DC gain, however, its maximum operating frequency is much less than the proposed one. In other word, the proposed structure delivers a larger gain bandwidth product value, which makes it more suitable for high frequency applications. The power supply rejection ratios (PSRR) of both

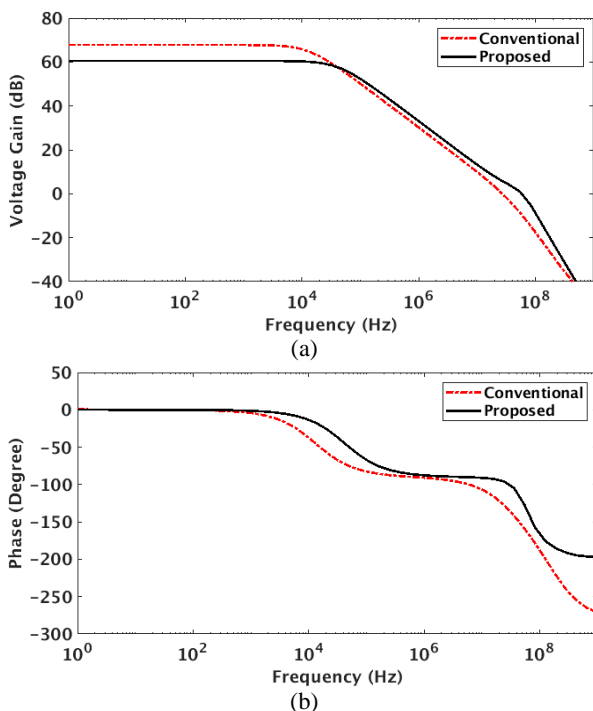


Fig. 7 The frequency behavior of the compensated amplifiers, a) amplitude, and b) phase (post-layout simulation).

amplifiers are compared in Fig. 8. As is shown, although the PSRR value of the proposed structure is less than that is of the traditional one in lower frequencies, but the PSRR of the traditional amplifier starts to roll off much faster, presenting much less PSRR than the proposed amplifier in higher operating frequencies (especially in Fig. 8 (a)). This, in fact, was predictable as it is the intrinsic disadvantage of the miller compensated amplifiers. The higher DC value of PSRR in traditional amplifier is due to its higher DC gain in this specific design.

The transient step response of the proposed amplifier is compared with the response of traditional amplifier in Fig. 9. As this figure shows, both of the amplifiers are stable and deliver fast rising and settling time. As is shown in Fig. 9, the proposed structure settles two times faster than the traditional amplifier.

To evaluate the robustness of the proposed structure against process uncertainties, the Monte Carlo simulation is performed to examine the two most important and vulnerable parameters, namely phase margin and DC gain. As is shown in the histograms of Fig. 10, the robustness of the proposed structure is acceptable, which assures its well-functionality after fabrication.

The important specifications of the proposed structure, incorporating the novel active feedback compensation scheme is compared with that is of the traditional miller compensated amplifier in Table 2. Examining Table 2 shows that the two amplifiers are almost the same in most of the parameters except the merits of gain bandwidth product and power consumption. In fact, the amplifier designed based on the proposed compensation

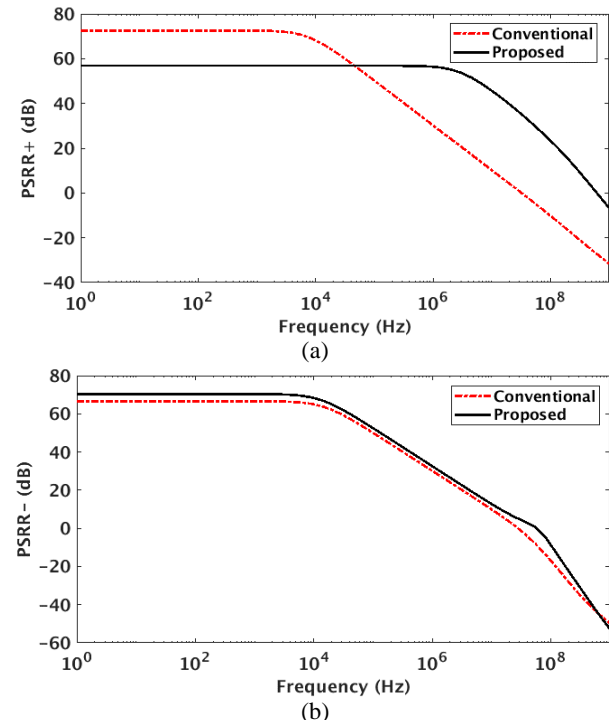


Fig. 8 The PSRR performance of the amplifiers, a) PSRR+, and b) PSRR- (post-layout simulation).

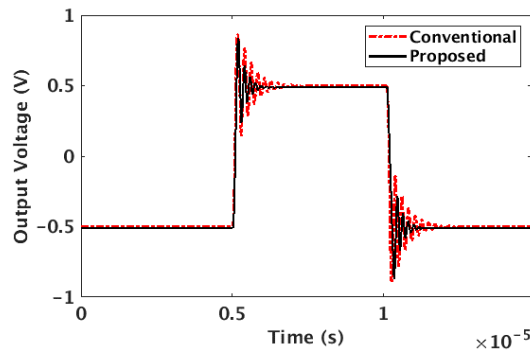


Fig. 9 The transient step response of the amplifiers (post-layout simulation).

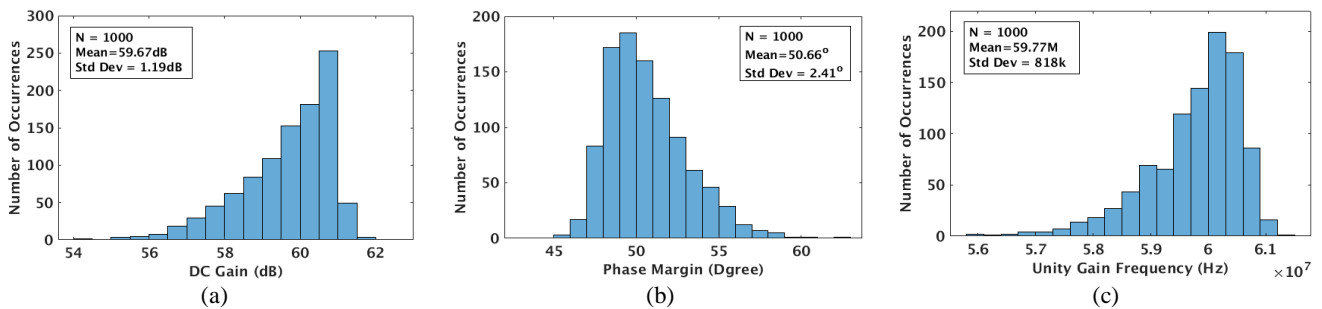


Fig. 10 The Monte Carlo analysis of the proposed amplifier, a) the DC gain, b) the phase margin, and c) the unity gain frequency (post-layout simulation).

Table 2 The specifications of the proposed amplifier versus those of the traditional scheme.

Parameters	Pre-Layout Simulation		Post-Layout Simulation	
	Traditional	Proposed	Traditional	Proposed
VDD (V)	1.8	1.8	1.8	1.8
Power (mW)	2.588	1.255	2.46	1.06
PSRR+ (dB)	72.7	59.1	72.6	56.9
PSRR- (dB)	83.7	70	66.6	70.38
Slew Rate (v/μs)	13.8	11.1	13.4	10.5
10% Settling Time (μs)	1	0.5	1.1	0.6
Gain (dB)	67	60	67.8	60.52
Phase Margin	51.1	50.8	49.45	49.54
Gain Bandwidth (MHz)	29.3	61.5	28.44	60.58
Load Capacitance (pF)	30	30	30	30

scheme delivers much more gain bandwidth product consuming much less power. This makes the proposed structure more power efficient and favorable for low power and high speed applications.

5 Conclusion

A novel active feedback frequency compensation scheme is presented in this work. The Spectre post layout simulations proved that a two-stage amplifier can be well-compensated based on the proposed active feedback frequency compensation scheme. The effectiveness of the proposed method is also verified through the mathematical formulations as well. The simulations were done utilizing TSMC 180nm CMOS standard technology. The Spectre post layout simulations showed that the proposed structure outperforms the traditional structure in terms of power consumption and gain bandwidth product. The robustness of the design was checked with Monte Carlo

simulations exhibiting acceptable results.

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H. Faraji Baghtash was born in Miandoab, Iran, in 1985. He received the B.Sc. degree from Urmia University in 2007, and M.Sc. and Ph.D. degrees both from Iran University of Science and Technology (IUST), Tehran, Iran in 2009, and 2014 in respectively, all in Electronics Engineering. He was with IUST Electronic Research Center Group, from 2007 to 2010 as a Researcher, and Science and Research Branch, Islamic Azad University from 2011 to 2015, as a Fellow Lecturer. He joined Sahand University of Technology, Tabriz, Iran as an Assistant Professor in 2015. He is the author or coauthor of more than 30 national and international papers and also collaborated in several research projects and has a registered Iranian patent. Dr. Faraji Baghtash was selected as distinguished researcher of the IUST in 2011. His current research interests include current mode/voltage mode analog integrated circuit design, low voltage, low power circuit and systems, analog microelectronics and digital system design.



Kh. Monfaredi received the B.Sc., M.Sc., and Ph.D. degrees from Tabriz University in 2001 and Iran University of Science and Technology (IUST) in 2003 and 2011, respectively. He was with Electronic Research Center Group, during 2001 to 2011 and was also an academic staff with Islamic Azad University, Miandoab Branch from 2006 to 2012. He

served as the Research and Educational Assistant of Miandoab Sama College from 2009 to 2011 and vice chancellor during 2011 to 2012. He is currently with Electrical and Electronics Engineering Faculty, Azarbaijan Shahid Madani University, Tabriz, Iran. He is the associate dean of engineering faculty, Azarbaijan Shahid Madani University since 2017. He is the author or coauthor of more than thirty national and international papers and also collaborated in several research projects. He is also the founder of electronic department in Islamic Azad University-Miyandoab Branch and was the chairman of 2010 electronic and computer scientific conference (ECSC2010) held in Islamic Azad University, Miandoab Branch. His current research interests include current mode integrated circuit design, low voltage, low power circuit and systems and analog microelectronics and data converters.



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