IUST
Iran University of Science and Technology

Iranian Journal of Electrical and Electronic Engineering

Journal Homepage: ijeee.iust.ac.ir

Research Paper

Design and Analysis of New Level Shifter With Gate Driver for Li-Ion Battery Charger in 180nm CMOS Technology

M. El Alaoui*(C.A), F. Farah*, K. El Khadiri*, H. Qjidaa*, A. Aarab*, A. Lakhssassi** and A. Tahiri***

Abstract: In this work, the design and analysis of new Level Shifter with Gate Driver for Li-Ion battery charger is proposed for high speed and low area in 180nm CMOS technology. The new proposed level shifter is used to raise the voltage level and significantly reduces transfer delay 1.3ns (transfer delay of conventional level shifter) to 0.15ns with the same input signal. Also, the level shifter with gate driver achieves a propagation delay of less than 0.25ns and the total area is only 0.05mm^2. The proposed level shifter with gate driver was designed, simulated and layouted in Cadence using TSMC 180nm CMOS technology.

Keywords: Li-Ion Battery Charger, Level Shifter, Gate Driver, Propagation Delay.

1 Introduction

AS we all know lithium is the lightweight metal and has a great electrochemical potential that leads Li-Ion batteries to get the higher energy density compared to other types of rechargeable batteries. Moreover, Li-Ion batteries offer significant advantages including low maintenance, great cell voltage, high discharge current, low internal resistance, and long lifespan. Although Ni-MH batteries and Ni-Cd batteries are among the rechargeable batteries, Li-Ion batteries are the most widely used and popular rechargeable batteries [1]. In the battery management integrated circuit, the most important element is the Li-Ion Battery charger that ensures the control safely of the charge without reducing its life [2, 3]. The Li-Ion battery chargers can be divided into two categories: the stand-alone chargers that are only utilized to charge battery packs and the embedded chargers are utilized inside the electronic devices, like smartphones, these embedded chargers must not only charge the batteries but also power the system [1]. For example, the integration of the dickson charge pump in the embedded chargers for programming on-chip an EEPROM to write a secret key [4]. It generates an output voltage to power the EEPROM according to a variable battery voltage Vbattery of the embedded chargers.

Fig. 1 shows the general architecture of the battery charger chip, it consists of several blocks: Constant Current (CC) control, Constant Voltage (CV) control, Level Shifter (L-S), Gate Driver (G-D), power MOS, current sensing circuit, bootstrap circuit and 5V LDO. In this work we presented the new L-S with G-D that we proposed to use in the battery charger chip and we compared our new proposed L-S with conventional L-S and other works [5-10] that are concerned with the use of level shifter in different domains and with different propagation delay that determine the speed of L-S, see Table 1 (Comparative analysis) in Section 3. Our new proposed L-S is more developed to raise the voltage level quickly and in a shorter propagation delay that equals 0.15ns.

The L-S is an essential circuit in multi-voltage systems. It is utilized between the input/output circuits and the central circuits. In literature, many designs for

Iranian Journal of Electrical and Electronic Engineering, 2019.
Paper first received 29 January 2019, revised 13 April 2019, and accepted 14 April 2019.
* The authors are with the Electronics, Signals, Systems and Computer Science Laboratory (LESSI), Department of Physics, Faculty of Sciences Dhar el Mehraz, Sidi Mohamed Ben Abdellah University, Fez, Morocco.
E-mails: mustapha.elalaoui@usmba.ac.ma, Fouad.farah@usmba.ac.ma, karim.elkhadiri@usmba.ac.ma, qjidah@yahoo.fr, and aarab_abdellah@yahoo.fr.
** The author is with the Department of Computer Science and Engineering, University of Quebec in Outaouais, (UQO) B-2014, Pavillon Lucien-Brault, Canada.
E-mail: ahmed.lakhssassi@uqo.ca.
*** The author is with the Laboratory of Computer Science and Interdisciplinary Physics, Sidi Mohamed Ben Abdellah University, ENS- Fez, Morocco.
E-mail: tahiri_ahmed@hotmail.com.
Corresponding Author: M. El Alaoui.

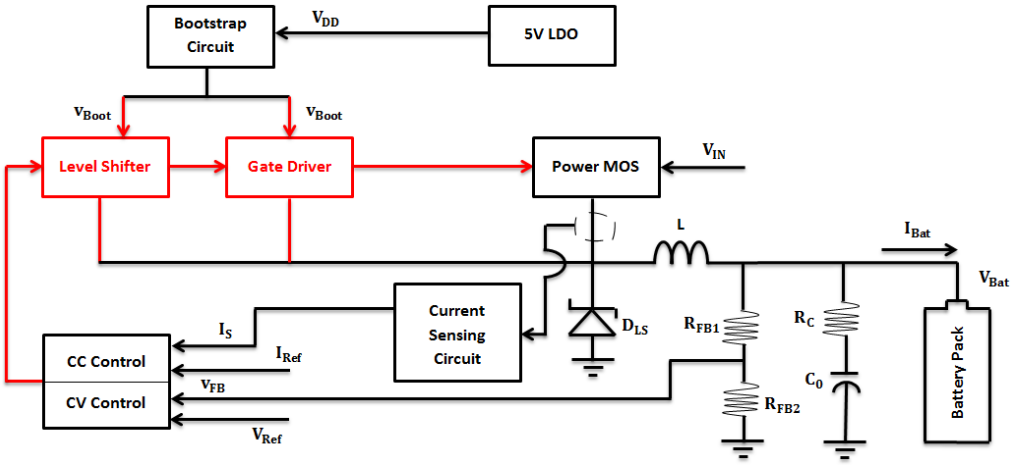

Fig. 1 The general architecture of the battery charger chip [1].

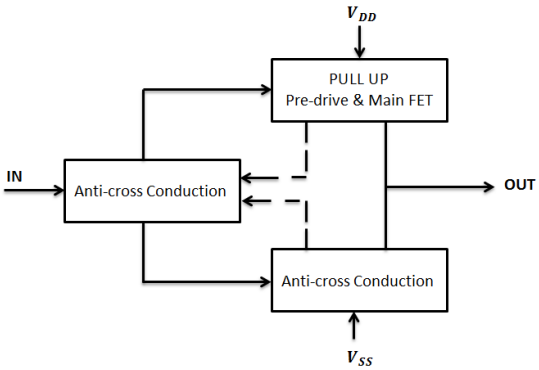

Fig. 2 The architecture of G-D [14].

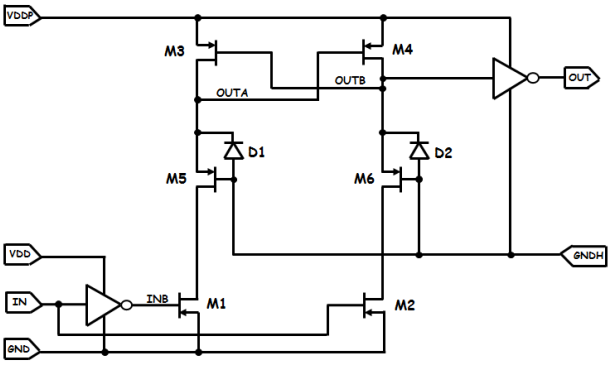

Fig. 3 Conventional L-S [13].

L-S has been indicated as dual and single supply [11]. The conventional L-S with high and low voltage supply VDDH, VDDL using 10 transistors has been registered [12]. It has a drawback of delay variation by dint of various transistors current driving capabilities, defeat at low supply core voltage VDDL and high power uptake [13].

Fig. 2 shows the architecture of G-D that consists of a pull-down and pull-up circuitries. The G-D is attached to the gate of a power MOS, which supplies power to the charge by switching actions. The gate capacitances can be reaching a couple of nF to large power MOSFETs. The anti-cross conduction circuit is requisite in the G-D to impede shoot through the power supply, from the pull-up circuit to the pull-down circuit, in order to control such an important gate capacity.

There are two sources of signal delay in the G-D, one owing to the anti-cross conduction circuit and the other to the pre-driver circuit. The anti-cross conduction circuit is too small because the minimum size devices are also utilized in the shoot-through protection circuit, and the pre-driver consists of a chain of the inverter [14]. We utilized in this paper a pre-driver to find a minimum signal delay by choosing the good number of gates and their neat size ratios.

We presented this article as the following: in Section 1 an Introduction; in Section 2 a presentation of the conventional and the proposed L-S; in Section 3 the simulation results of the conventional and proposed L-S with a comparison between them and other works, along with another simulation results of the new proposed L-S with G-D; and in Section 4 a conclusion.

2 Level-Shifter

The L-S is utilized to convert low voltage level to high voltage level or the opposite. Translator circuits and Bi-directional L-S are utilized to interface between input-output voltage levels and applications with different supply voltage. L-S is the decks that convert from low core voltage to high voltage. There are many types of L-S like dual supply L-S and single supply L-S. The single supply L-S allows communication between modules without adding all extra supply pin; it has an advantage over the dual supply L-S in terms of the pins number, obstruction in the global cost of the system and routing [15].

2.1 Conventional Level-Shifter

Fig. 3 shows conventional L-S. It is a half-lock type that is made by two PMOS M3, M4 and two NMOS M1, M2. This device is controlled by low voltage VIN and its complements. As the VIN passage from low to high voltage, the M1 will be ON and M2 is OFF, so that

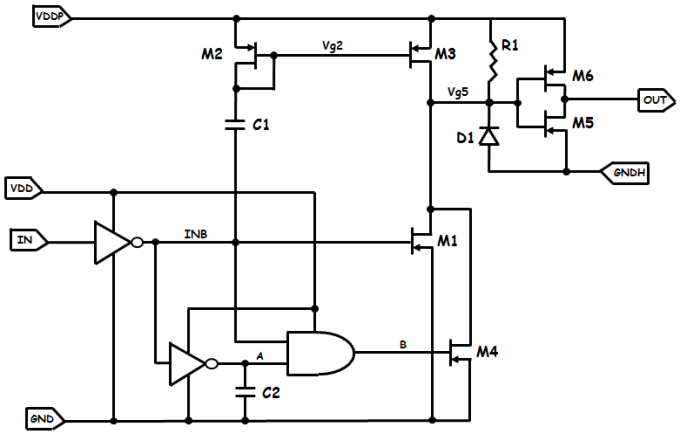

Fig. 4 The new proposed L-S.

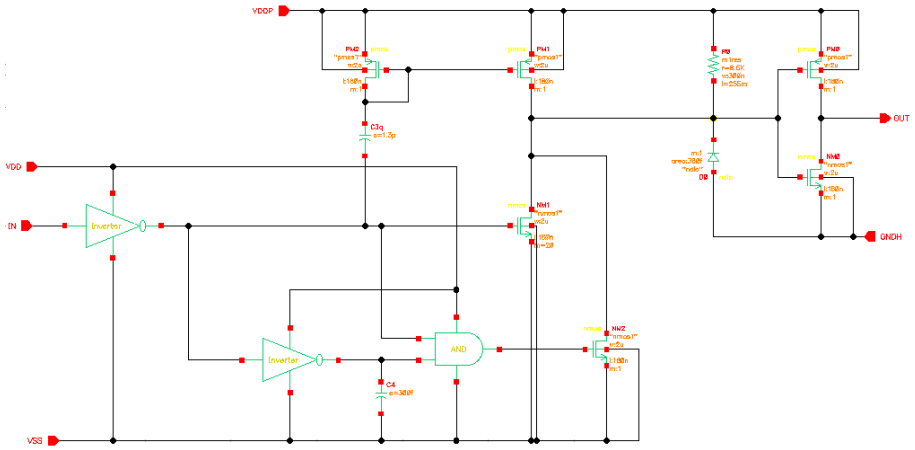

Fig. 5 Schematic of proposed level shifter under CADENCE software.

the node voltage OUTA is pulled down and the node voltage OUTB is pulled up, lead to M4: ON and M3: OFF. Whenever M4 is ON the voltage at OUTB will be even to VDDP and M3 will be OFF, and the voltage at OUTA remains discharged. There can be impedance trouble between the devices. Therefore, pull up and pull-down network forces must be accurately balanced and reduced to sustain the required logic levels [16]. It is troublesome to realize when the level shifting signals are at a voltage level below the threshold [17].

2.2 New proposed Level-Shifter

The new proposed L-S is shown in Fig. 4, comprises of four devices in total with capacity C1 and resistance R1, in which two transistors are NMOS type namely M1, M4 make leveling upshift and two transistors are PMOS type namely M2, M3. Falling input signal couples through C1 to discharge Vg2 node in high-low transition. When M3 is ON momentarily R1 pulls up Vg5 and is already OFF when rising input. The transistor NMOS type namely M1 pulls Vg5 node down.

Diode connected b/w GNDP and Vg5, Protect Vsg of transistor NMOS type namely M5 when Vg5 is pulled low and GNDP node is rising high following VIN.

If we reduce the size of transistor NMOS type namely M1, It will consequently reduce the current and the charge, but small M1 may not allow Vg5 node to be pulled down.

The high out storage charge built across the diode when Vg5 is low, when out in high-to-Low transition, the charge needed to be removed to pull Vg5 node up to BOOT, and that can be a risk of a huge propagation delay.

Minimum propagation delay is a function of 3 things: process technology, operating voltage and of course: circuit design.

The equation of propagation time is:

$$i = C\frac{dv}{dt} = C_{ox}.W.L\frac{dv}{dt} \tag{1}$$

and

$$I = \frac{\mu_n C_{ox}}{L} \times \frac{W}{L}\left(V_{gs} - V_{th}\right)^2 \tag{2}$$

so,

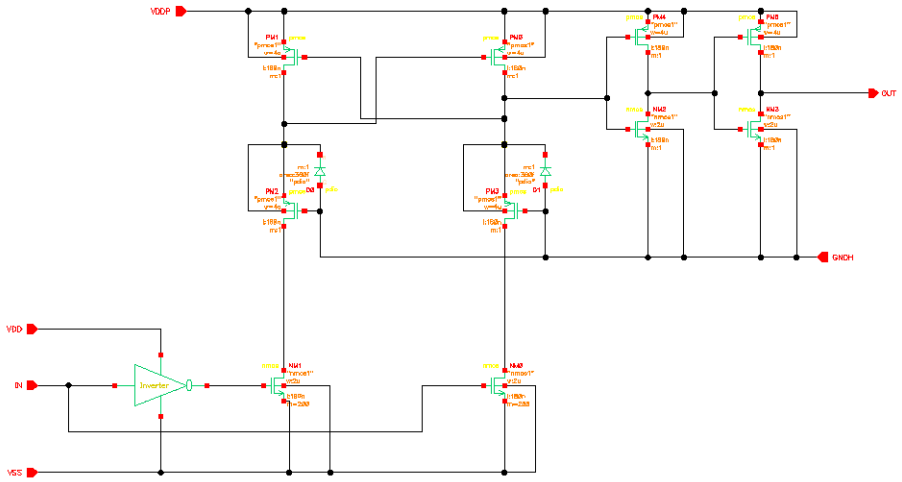

Fig. 6 Schematic of conventional level shifter under CADENCE software.

$$t_p \approx \frac{2C_{ox}W.L^2.V_{DD}}{\mu_n C_{ox} {V_{DD}}^2} \approx \frac{2L^2}{\mu_n {V_{DD}}^2} \quad (3)$$

Higher VDD with quicker transition time give faster de-coupling and give also higher speed.

3 Simulation Results

3.1 Simulation Result of Proposed Level Shifter and Conventional Level Shifter

Fig. 5 shows schematic of proposed L-S and Fig. 6 shows schematic of conventional L-S, under CADENCE software.

Fig. 7 show the waveform than transient analysis of proposed L-S and conventional L-S.

VDD and VDDP are the supply voltages used in this circuit. VDD is given as 1.8V and VDDP is given as 5V. The proposed L-S circuit and the conventional L-S circuit make shifting operation from 1.8V to 5V. The output of 5V was obtained according to an input pulse of 1.8V. They are designed using 180nm CMOS technology under CADENCE software. The stable output of proposed L-S can be viewed in Fig. 7(a).

We can observe from Figs. 7(b) and 7(c), the transfer delays of the proposed L-S and the conventional L-S. The results show that the proposed L-S significantly reduces transfer delay 1.3ns (transfer delay of conventional L-S) to 0.15ns with the same input signal.

Table 1 is a comparative analysis between proposed L-S and other works/references.

3.2 Monte Carlo Simulation of Proposed Level Shifter and Conventional Level Shifter

Monte Carlo simulation is concerned with studying how the individual devices mismatches of a circuit may assemble and impact the circuit.

Fig. 8 shows the histogram of the difference in time delay of the conventional L-S and Fig. 9 shows the

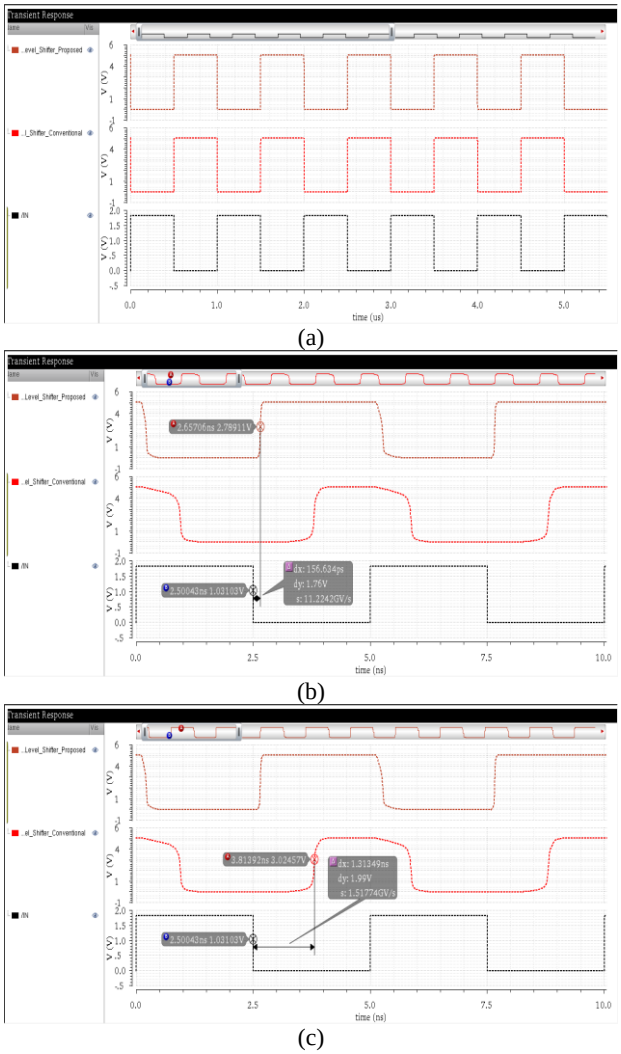

Fig. 7 Waveforms: a) Transient analysis of proposed level shifter and conventional level shifter, b) Transfer delays of proposed level shifter, and c) Transfer delays of conventional level shifter.

Table 1 Comparative analysis.

Work/Reference	Technology	VDDL [V]	VDDH [V]	Delay [ns]
This Work	180nm CMOS	1.8	5	0.15
[5]	65 nm CMOS	1.2	5	0.61
[6]	180nm CMOS	0.4	3	15.65
[7]	0.35um HV	3.3	6.7-10	3
[8]	90nm CMOS	0.2	1	10.99
[9]	45nm CMOS	0.7	1.2	12.18
[10]	28nm FDSOI	0.25	1	3.11

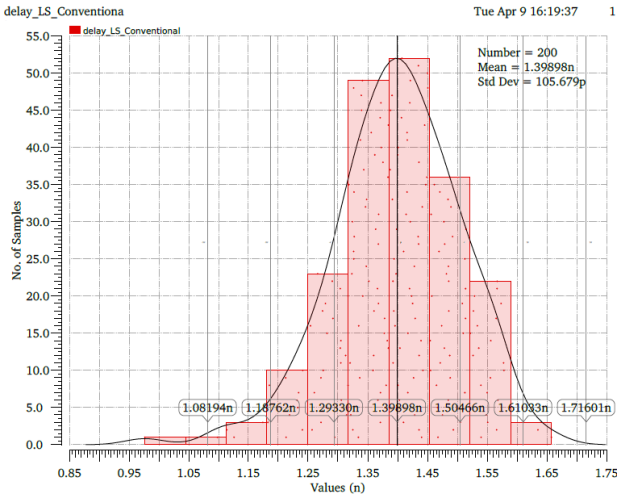

Fig. 8 Histogram of the difference in time delay of the conventional L-S.

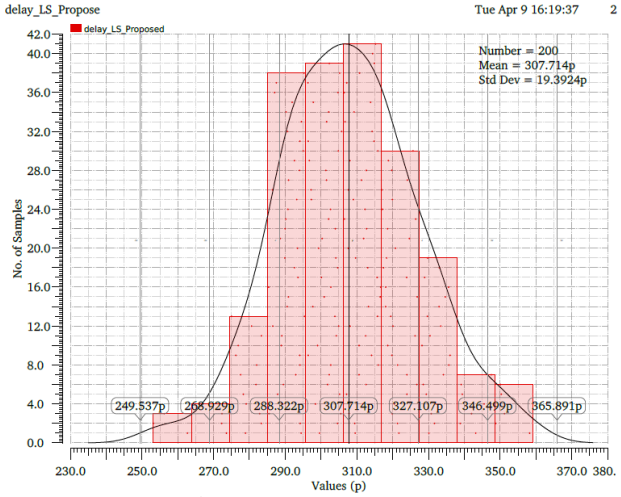

Fig. 9 Histogram of the difference in time delay of the proposed L-S.

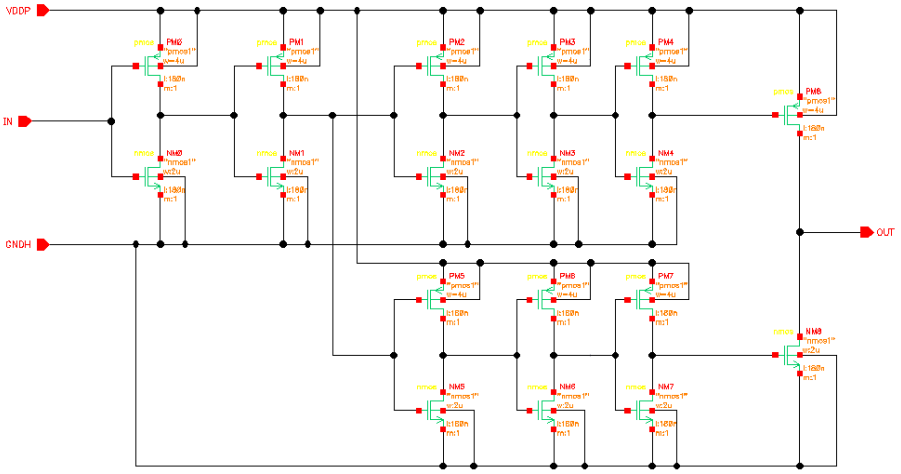

Fig. 10 Schematic of G-D under CADENCE software.

histogram of the difference in time delay of the proposed L-S, we can observe from Monte Carlo simulation the standard deviation of the conventional L-S for 200 simulations was 105.679ps, while the standard deviation of the proposed L-S for 200 simulations was 19.3924ps.

3.3 Simulation Result of Proposed Level Shifter With Gate Driver

Fig. 10 shows a schematic of G-D and Fig. 11 shows a schematic of the proposed L-S with G-D, under CADENCE software.

Fig. 12 show the transient analysis of proposed L-S with G-D that we used in our battery charger chip, under CADENCE software.

The proposed L-S with G-D makes shifting operation from 1.8V to 5V. The output of 5V was obtained according to an input pulse of 1.8V. It is designed using an 180nm CMOS technology under CADENCE software. The stable output of proposed L-S with G-D can be viewed in Fig. 12. For the simulation, the rise time is approximately 36ps, the fall time is almost 36ps, and the delay time is round 0.25ns.

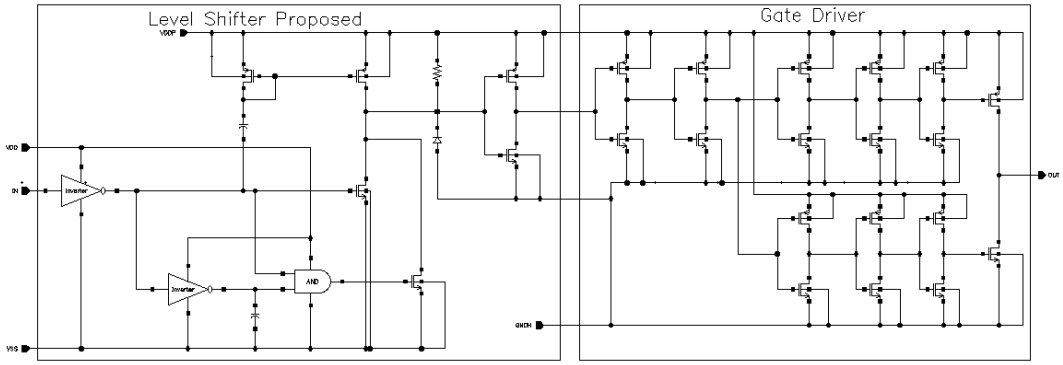

Fig. 11 Schematic of the proposed L-S with G-D under CADENCE software.

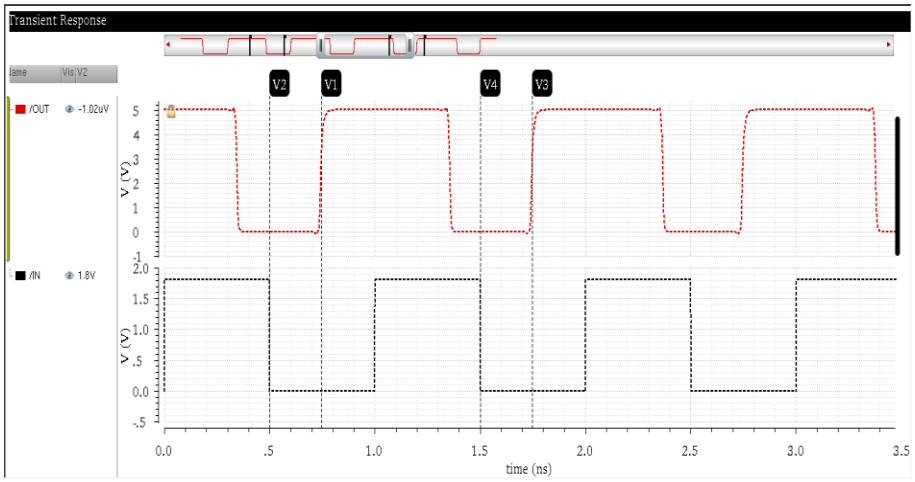

Fig. 12 The transient analysis of proposed L-S with G-D.

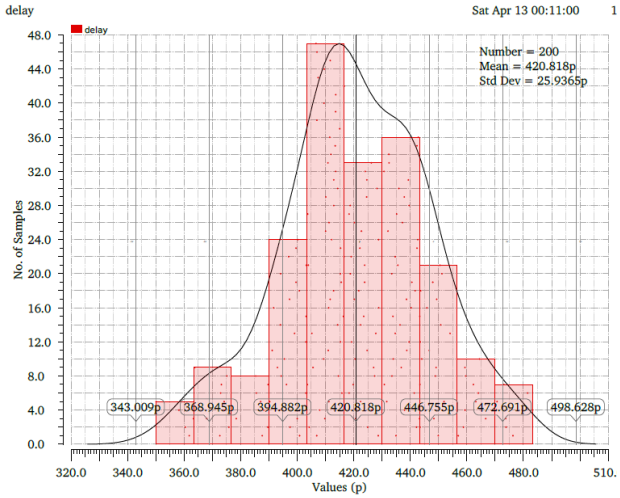

Fig. 13 Histogram of the difference in time delay of the proposed L-S with G-D.

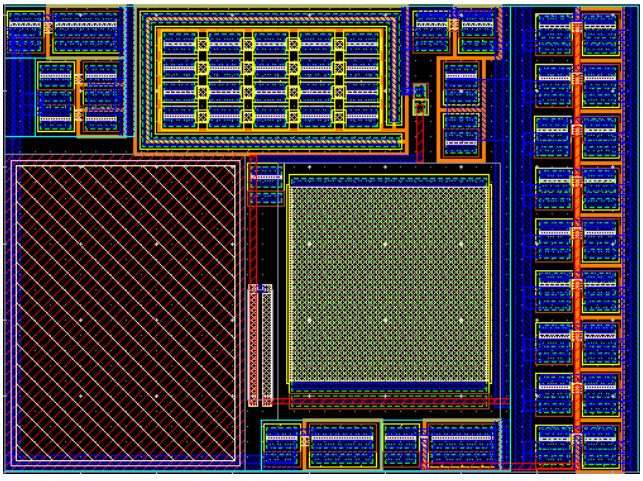

Fig. 14 Layout of the proposed L-S with G-D.

3.4 Monte Carlo Simulation of proposed Level Shifter With Gate Driver

Fig. 13 shows the histogram of the difference in time delay of the proposed L-S with G-D, we can observe from Monte Carlo simulation the standard deviation for 200 simulations was 25.9365ps.

3.5 Layout

The layout for the proposed L-S with G-D for Li-Ion battery charger is shown in Fig. 14. All devices or circuits prone to produce electromagnetic interference or susceptible to interference are enclosed with double layer guard rings. The layout is done by respecting following items; design rules (DRM, MRC and Density) and designer constraints information (constraint manager, match Cat, text, etc.). Layout is occupying a total area of 0.05mm^2.

4 Conclusion

A low cost, low size and high-speed L-S with G-D for

Li-Ion battery charger have been successfully designed and implemented in TSMC 180 nm CMOS process. Circuit design, simulation, analysis and layout design are all included in this study. The proposed L-S significantly reduces transfer delay 1.3ns (transfer delay of conventional L-S) to 0.15ns with the same input signal. The proposed L-S with G-D achieves a propagation delay of 0.25ns and the total area is only 0.05 mm^2.

Acknowledgement

This work was supported by the National Center for Scientific and Technical Research (CNRST Morocco) under the PPR2 program.

References

[1] J. F. Wu, C. L. Wei, and Y. Z. Juang, "A monolithic high-voltage Li-Ion battery charger with sharp mode transition and partial current control technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 65, No. 9, pp. 3099–3109, Sep. 2018.

[2] F. Farah, M. El Alaoui, K. El Khadiri, and H. Qjidaa, "New analog Li-Ion battery charger using pulsed charging method," in *6th International Conference on Multimedia Computing and Systems (ICMCS)*, pp. 10–12, May 2018.

[3] K. El Khadiri, H. Akhmal, and H. Qjidaa, "Li-Ion battery charging with a buck-boost DC–DC converter for a portable device power management," *Journal of Low Power Electronics*, Vol. 13, No. 2, pp. 263–270, Jun. 2017.

[4] M. El Alaoui, F. Farah, K. El Khadiri, H. Qjidaa, A. Aarab, R. EL Alami, and A. Lakhssassi "Analysis and design of dickson charge pump for EEPROM in 180nm CMOS technology," in *International Conference on Intelligent Systems and Computer Vision (ISCV)*, pp. 1–5, 2–4 Apr. 2018.

[5] G. Maderbacher, T. Jackum, W. Pribyl, S. Michaelis, D. Michaelis, and C. Sandner, "Fast and robust level shifters in 65 nm CMOS," in *Proceedings of the ESSCIRC (ESSCIRC)*, pp. 195–198, 2011.

[6] N. B. Romli, M. Mamun, M. A. Sobhan, and H. Husain, "design of a low Power dissipation and low input voltage range level shifter in Cedec 0.18-µm CMOS process," *World Applied Sciences Journal*, Vol. 19, No. 8, pp 1140–1148, Aug. 2012.

[7] Y. Moghe, T. Lehmann, and T. Piessens, "Nanosecond delay floating high voltage level shifters in a 0.35µm HV-CMOS technology," *IEEE Journal of Solid-State Circuits*, Vol. 46, No. 2, Feb. 2011.

[8] P. Gosatwar and U. Ghodeswar, "Design of voltage level shifter for multi-supply voltage design," in *International Conference on Communication and Signal Processing (ICCSP)*, pp. 0853–0857, 6–8 Apr. 2016.

[9] M. Vaidya, A. Naugarhiya, and S. Verma, "High speed bootstrapping generic voltage level shifter," in *Second International Conference on Advances in Electronics, Computers and Communications (ICAECC)*, pp. 1–4, 9–10 Feb. 2018.

[10] S. Chatterjee and U. Rückert, "Scaling down a level shifter circuit in 28 nm FDSOI technology," in *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, pp. 1–4, 19–21 Mar. 2018.

[11] P. Liu, X. Wang, D. Wu, Z. Zhang, and L. Pan, "A novel high-speed and low-power negative voltage level shifter for low voltage applications," in *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 601–604, 30 May 2010.

[12] S. C. Tan and X. W. Sun, "Low power CMOS level shifters by bootstrapping technique," *Electronics Letters*,Vol. 38, No. 16, Aug. 2002.

[13] K. H. Koo, J. H. Seo, M. L. Ko, and J. W. Kim, "A new level-up shifter for high speed and wide range interface in ultra-deep sub-micron," in *IEEE International Symposium on Circuits and Systems*, pp. 1063–1065, 2005.

[14] M. R. Hoque and S. S Ang, "Design technique of an integrated gate driver," in *Proceedings of the World Congress on Engineering and Computer Science 2008 (WCECS 2008)*, San Francisco, USA, 22–24 Oct. 2008.

[15] S. Vaishnavi, S. Ashok, and T. Abbas, "Design and analysis of level shifter in high voltage transmitter," *International Journal of Scientific and Research Publications*, Vol. 4, No. 1, Jan. 2014.

[16] S. Gundala, V. K. Ramanaiah, and P. Kesari, "Nanosecond delay level shifter with logic level correction," in *International Conference on Advances in Electronics Computers and Communications*, pp. 1–5, 2014.

[17] B. Zhai, S. Pant, L. Nazhandali, S. Hanson, J. Olson, A. Reeves, M. Minuth, R. Helfand, T. Austin, D. Sylvester, and D. Blaauw, "Energy-efficient subthreshold processor design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 8, pp. 1127–1137, Aug. 2009.

M. El Alaoui Received his Master degree in Microelectronics from faculty of sciences Dhar EL Mahraz Fez Morocco, in 2017. He is now Ph.D. student in the Department of Physics Sidi Mohammed Ben Abdellah University, Fez, Morocco LESSI laboratory. His main research interest includes renewable energy, switch modeaudio amplifier, CMOS mixed mode integrated circuit design, design techniques for RFID, Li-Ion battery charger and power management.

F. Farah Received his Master degree in Microelectronics from faculty of sciences Dhar EL Mahraz Fez Morocco in 2016. He is now Ph.D. student in the Department of Physics Sidi Mohammed Ben Abdellah University, Fez, Morocco LESSI laboratory. His main research interest includes renewable energy, switch mode audio amplifier, CMOS mixed mode integrated circuit design, design techniques for RFID, Li-Ion battery charger and power management.

K. El Khadiri was born in Fez, Morocco in 1978. He received M.Sc. and Ph.D. degrees in Faculty of Sciences from Sidi Mohammed Ben Abdellah University in 2011 and 2017, respectively. Since 2012, he served as a Research Scientist at Faculty of Science in the University of Sidi Mohammed Ben Abdellah, Fez, Morocco and Guest Researcher at LIMA laboratory in UQO Canada. His current interests include switch mode audio amplifier, CMOS mixed-mode integrated circuit design, design techniques for RFID, RF front-ends for passive tags, Li-Ion battery charger and power management.

H. Qjidaa received the M.Sc. and Ph.D. degrees in Electrical Engineering from Nuclear Physics Institute of Lyon, in France 1984 and 1987, respectively. Since 1987, he served as a Research Scientist at Faculty of Science in the University of Sidi Mohammed Ben Abdellah, Fez, Morocco. He has been a Professor with the Department of Physics. He is currently also a Director of the Information Analysis and Micro-system Teams (IAMS), and Vice Director of the electronic signal and systems laboratory (LESSI). His current research interests are in image processing, pattern recognition, data analysis, machine intelligence, low-power circuit design techniques for RFID, RF front- ends for passive tags, and CMOS mixed-mode integrated circuit design.

A. Aarab is Professor at the Faculty of Sciences, University of Sidi Mohammed Ben Abdellah, Fez, Morocco. He received his "Doctorate of 3rd cycle" degree from the University of Pau, France, in 1982, and "State thesis" degree in 1999 from University Sidi Mohamed Ben Abdellah, Fez, Morocco. His research areas include, image processing, information retrieval and industrial applications.

A. Lakhssassi is Professor at the Department of Computer Science and Engineering University of Quebec in Outaouais, He is specializes in energy sciences and thermal aspects in integrated circuits. He is responsible for the Advanced Microsystems Engineering Laboratory, which focuses on microelectronics and thermal aspects in VLSI Microsystems. Professor Lakhssassi heads the Advanced Microsystems Engineering Laboratory (LIMA) whose research work in the field of microelectronics and SoCs (System-on-Chip) allows UQO to actively participate in the ReSMiQ center (Regroupement Strategic Microsystems of Quebec) funded by the FRQNT. This strategic cluster is in fact the largest research center in Quebec in the field of microelectronics and its applications. A good example of his collaborations is in the biomedical field of diagnostics with thermal camera image processing and bio-implantable chip design. His main research interest includes Electronic, Electromagnetism, Thermal aspects, Numerical methods, Energy sciences, electrothermics, Constraints and distortions, Materials sciences.

A. Tahiri received the graduate degree DES in Department of Physics, Sidi Mohammed Ben Abdellah University, Morocco in 1997, received the Ph.D. degree in Physics from the University Sidi Mohamed Ben Abdellah, Faculty of Science, Morocco in 2005. He completed his doctoral studies in didactics of science in the University of Sherbrooke in Canada in 2010. He is now a Professor in Superior Normal School, ENS-FEZ, Morocco. His research interests include image processing, computer science and didactics of scientific disciplines.