

A Current-Mode Single-Resistance-Controlled Oscillator Employing VDCC and All Grounded Passive Elements

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Abstract: Realization of a novel single-resistance-controlled oscillator, employing an active element and all grounded passive elements, is the purpose of this manuscript. With requirements for completing the design being only a single Voltage Differencing Current Conveyor and four grounded passive components, it is also a preferable choice for integrated circuit implementation. The designed circuit has an independent control of the frequency of oscillation and current mode output can be achieved from high impedance port, explicitly. Simulation results are presented using PSPICE software along with the regular mathematical analysis. At last experimental verification of the proposed circuit is shown using commercially available integrated circuits.

Keywords: Active Devices, Current Mode Circuits, Quadrature Oscillator, Voltage Differencing Current Conveyor, Sinusoidal Oscillator.

1 Introduction

THERE is an inevitable competition between voltage-mode (VM) and current-mode (CM) circuits. The current-mode circuits have advantages over voltage mode circuits like higher bandwidth, low power consumption, low component count, etc. [1]. Sinusoidal oscillators are the essential and elementary units for analog signal processing operations whose applications can easily be found in the soil measurement system, zero-IF and image-reject receivers, etc. [2, 3]. The purpose of sinusoidal oscillators is to generate a sinusoidal waveform, whose combination can be converted into any of a periodic signal and can be analyzed mathematically with the help of the Fourier series [4].

The design of sinusoidal oscillator using different active building blocks (ABBs) such as, current differencing buffered amplifier (CDBA) [5, 6], third generation current conveyor (CCIII) [7, 8], differential voltage complementary current conveyor (DVCCC) [9,

10], four-terminal floating nullor (FTFN) [11], modified current differencing transconductance amplifier (MCDTA) [12], operational trans-resistance amplifier (OTRA) [13, 14], plus type second generation current conveyor (CCII+) [15], fully differential current conveyor (FDCCII) [16], differential difference current conveyors feedback amplifier (DDCCFA) [17], differential input and buffered transconductance amplifier (DBTA) [18], inverting second generation current conveyor (ICCI) [19], differential difference current conveyors (DDCC) [20], voltage differencing current conveyor (VDCC) [21-28] is already there in open literature. Single-resistance-controlled oscillator (SRCO) is a special class of the waveform generator where the condition of oscillation (CO) and frequency of oscillation (FO) can be controlled through a single passive resistor. The task of designing a pure sinusoidal oscillator includes the employment of a minimum number of active and passive elements, use of grounded/floating passive components, provision of explicit current outputs, and flexibility of having independent CO and FO and so on. The detailed compendium of the features of the existing SRCOs in comparison with the proposed circuit is shown in Table 1. It is worth noting here that only such oscillator circuits have been taken into consideration where only single active device is sufficient to make the complete design.

Here in the manuscript, the author presents one such

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Table 1 Comparison of salient characteristics of already published sinusoidal oscillators

S.No.	Ref. No	Active device	No of passive elements	All grounded passive components	Availability of explicit output	Independent FO
1	[9]	DVCC	5	No	Yes	Yes
2	[10]	DVCC	5	No	Yes	Yes
3	[11]	FTFN	5	No	No	Yes
4	[12]	MCDTA	4	No	Yes	Yes
5	[13]	OTRA	5	No	Yes	Yes
6	[14]	OTRA	5	No	Yes	No
7	[15]	CCII+	5	No	No	Yes
8	[16]	FDCCH	5	Yes	Yes	Yes
9	[17]	DDCCFA	5	No	Yes	Yes
10	[18]	DBTA	5	Yes	Yes	Yes
11	[19] (Fig. 2)	ICCH	5	No	No	Yes
12	[20]	DDCC	4	No	Yes	No
Proposed Circuit		VDCC	4	Yes	Yes	Yes

oscillator circuit that employs only a single active element along with all grounded passive components. The designed oscillator circuit provides explicit current output from its high impedance port and its FO can be independently controlled, i.e., without affecting CO, through a grounded passive resistor. The feasibility of the derived circuit is validated with the help of software simulations as well as hardware experimental results, which are incorporated in the manuscript.

The entire paper is further partite into 6 segments. In the upcoming section, the proposed design with ideal mathematical analysis is provided. The non-ideal and sensitivity are represented in Section 3. Another imperative mathematical calculation, i.e., parasitic analysis is mentioned in Section 4. The design has been practically validated in two sections, where Section 5 includes simulation results and Section 6 demonstrates the experimental results. At last, the manuscript is summarized with the conclusion.

2 Proposed Circuit

In 2009, Biolek et. al. proposed a novel versatile active element named as Voltage Differencing Current Conveyor (VDCC) [29]. It is composed of two distinct ABBs, i.e., OTA (operational transconductance amplifier) and CCII (second generation current conveyor). The fixed hardwired connection between these two sub-blocks makes complete design more versatile. Fig. 1 shows the block diagram of the active element. The characteristic equation of ideal VDCC is given in (1).

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix} \tag{1}$$

The proposed circuit of SRCO that employs few

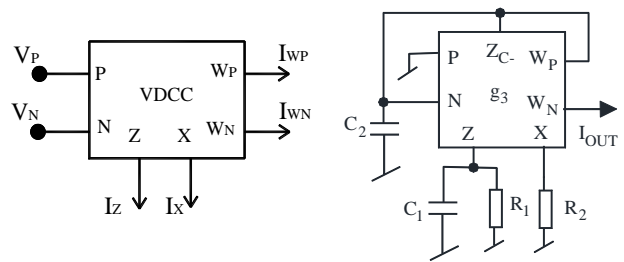


Fig. 1 Block Diagram of VDCC [21].

Fig. 2 Proposed SRCO employing VDCC.

passive elements and a single VDCC is delineated in Fig. 2. It can be easily visualized from Fig. 2 that the given oscillator utilizes only grounded passive elements, along with the feature of providing explicit output from its high impedance port. To get the mathematical model of the proposed oscillator, the characteristic equation of VDCC is applied to the circuit. By opting simple circuit fundamentals, the characteristic equation of designed SRCO comes out as given by (2). The two conditions, mathematically responsible for re-producing the oscillations, i.e., CO and FO are presented in (3) and (4).

$$s^2 + s \left[\frac{1}{C_1 R_1} - \frac{g_3}{C_2} \right] + \frac{g_3}{C_1 C_2} \left[\frac{1}{R_2} - \frac{1}{R_1} \right] = 0 \tag{2}$$

$$\text{CO: If } C_1 = C_2, \frac{1}{R_1} - g_3 = 0 \tag{3}$$

$$\text{FO: } \omega_0 = \sqrt{\frac{g_3}{C_1 C_2} \left[\frac{1}{R_2} - \frac{1}{R_1} \right]} \tag{4}$$

It is evident from (4) that the wide swing in the oscillation frequency can be easily achieved, without altering the oscillation condition, by changing the value of the grounded passive resistance R_2 . On the other hand, the oscillation condition can also be orthogonally set, with the help of grounded resistor R_1 .

3 Non-Ideal and Sensitivity Analysis

Before this section, all the analysis and calculations,

to get the desirable mathematical outcomes, were performed considering the active element an ideal block. Once the focus shifts to the non-idealities of the active device, equations get changed. The non-ideal, characteristic equation of the VDCC, is represented by (5). By applying the simple fundamentals of network analysis and using (5) in it, on the proposed oscillator circuit, new equations emerge, as given by (6)-(8). The non-ideal characteristic equation of the derived oscillator is given by (6) whereas CO and FO including non-ideal impact of the device are presented by (7) and (8).

$$\left. \begin{aligned} I_z &= \alpha \cdot g_m (V_p - V_N) \\ V_z &= \beta V_x \\ I_{WP} &= \gamma_P I_x \\ I_{WN} &= -\gamma_N I_x \end{aligned} \right\} \quad (5)$$

$$s^2 + s \left[\frac{1}{C_1 R_1} - \frac{\alpha g_3}{C_2} \right] + \frac{\alpha g_3}{C_1 C_2} \left[\frac{\beta \gamma_{WP}}{R_2} - \frac{1}{R_1} \right] = 0 \quad (6)$$

$$\text{CO: } \frac{1}{C_1 R_1} - \frac{\alpha g_3}{C_2} = 0 \quad (7)$$

$$\text{FO: } \tilde{\omega}_0 = \sqrt{\frac{\alpha g_3}{C_1 C_2} \left[\frac{\beta \gamma_{WP}}{R_2} - \frac{1}{R_1} \right]} \quad (8)$$

By inspection of the equations, i.e., (6)-(8), it is perceivable that there is not much deviation between the ideal and non-ideal behavior of the oscillator, thus justifying the design example.

The sensitivity performance of the derived SRCO has been accounted by analyzing the sensitivity of frequency of oscillation, towards passive elements and trans-conductance gain. This analysis has been derived for both, ideal and non-ideal frequency. The variations in ideal FO has been provided by (9)-(11), whereas the same for non-ideal FO has been shown in (12)-(14). The sensitivity measure of non-ideal FO also includes non-ideal parameters, i.e., α , β , and γ_{WP} , given in (15).

$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2} \quad (9)$$

$$S_{g_3}^{\omega_0} = \frac{1}{2} \quad (10)$$

$$\left. \begin{aligned} S_{R_2}^{\omega_0} &= -\frac{1}{2} \left[\frac{\frac{g_3}{C_1 C_2 R_2}}{\frac{g_3}{C_1 C_2} \left(\frac{1}{R_2} - \frac{1}{R_1} \right)} \right] \\ S_{R_1}^{\omega_0} &= \frac{1}{2} \left[\frac{\frac{g_3}{C_1 C_2 R_1}}{\frac{g_3}{C_1 C_2} \left(\frac{1}{R_2} - \frac{1}{R_1} \right)} \right] \end{aligned} \right\} \quad (11)$$

$$S_{C_1}^{\tilde{\omega}_0} = S_{C_2}^{\tilde{\omega}_0} = -\frac{1}{2} \quad (12)$$

$$S_{g_3}^{\tilde{\omega}_0} = \frac{1}{2} \quad (13)$$

$$S_{R_1}^{\tilde{\omega}_0} = \frac{1}{2} \left[\frac{\frac{\alpha \cdot g_3}{C_1 C_2 R_1}}{\frac{\alpha \cdot \beta \cdot \gamma_{WP} \cdot g_3}{C_1 C_2 R_2} - \frac{\alpha \cdot g_3}{C_1 C_2 R_1}} \right] \quad (14)$$

$$S_{R_2}^{\tilde{\omega}_0} = -\frac{1}{2} \left[\frac{\frac{\alpha \cdot \beta \cdot \gamma_{WP} \cdot g_3}{C_1 C_2 R_2}}{\frac{\alpha \cdot \beta \cdot \gamma_{WP} \cdot g_3}{C_1 C_2 R_2} - \frac{\alpha \cdot g_3}{C_1 C_2 R_1}} \right]$$

$$S_{\alpha}^{\tilde{\omega}_0} = \frac{1}{2}$$

$$S_{\beta}^{\tilde{\omega}_0} = S_{\gamma_{WP}}^{\tilde{\omega}_0} = \frac{1}{2} \left[\frac{\frac{\alpha \cdot \beta \cdot \gamma_{WP} \cdot g_3}{C_1 C_2 R_2}}{\frac{\alpha \cdot \beta \cdot \gamma_{WP} \cdot g_3}{C_1 C_2 R_2} - \frac{\alpha \cdot g_3}{C_1 C_2 R_1}} \right] \quad (15)$$

Above solved equations, (9)-(15) reflect that the non-ideal factors of the device does not influence much the functioning of the designed SRCO as all the sensitivity calculations are under permissible limits, i.e., from -1 to 1.

4 Parasitic Analysis

This section of the manuscript shows the effects of the parasitics on the proposed circuit. A well-known block diagram of VDCC, under the influence of device parasitics, is shown in Fig. 3 [21]. When the block of VDCC, used in Fig. 2, is replaced by this parasitic block, a new circuit diagram comes into existence, shown in Fig. 4. The device parasitic resistance R_x comes in series with the grounded resistance R_2 and its effect gets diluted by external passive resistor. Similarly, the parallel parasitic resistance that appears across Z terminal gets merged with R_1 . The capacitive parasitic element, i.e., C_p gets neglected in presence of physical external grounded capacitor, i.e., C_2 . In order to avoid convoluted mathematical analysis, some assumptions and simplifications have been taken into considerations. The cumulative effect of parallel resistance of W_p and R_c - terminals, is reflected by R_b , in Fig. 4.

Assumptions and simplifications

$$\left. \begin{aligned} R_a &= R_1 \parallel R_z \\ R_2 &\gg R_x \\ R_b &= R_p \parallel R_{zc-} \\ C_2 &\gg C_p \end{aligned} \right\} \quad (16)$$

The second-order characteristic equation of the derived sinusoidal oscillator is presented in (17). The

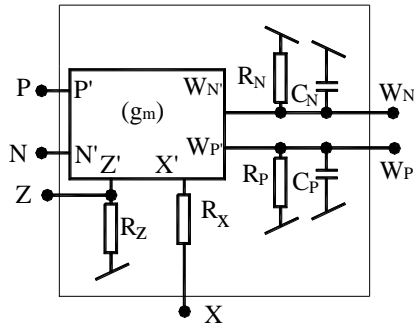


Fig. 3 Block diagram of the VDCC under the influence of device parasitics [21].

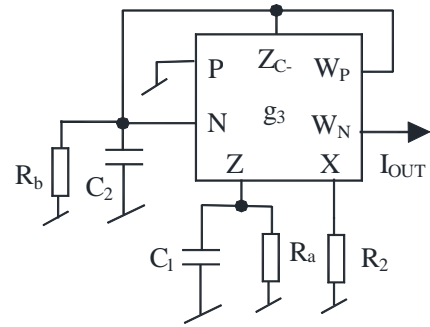


Fig. 4 Proposed oscillator including device parasitics.

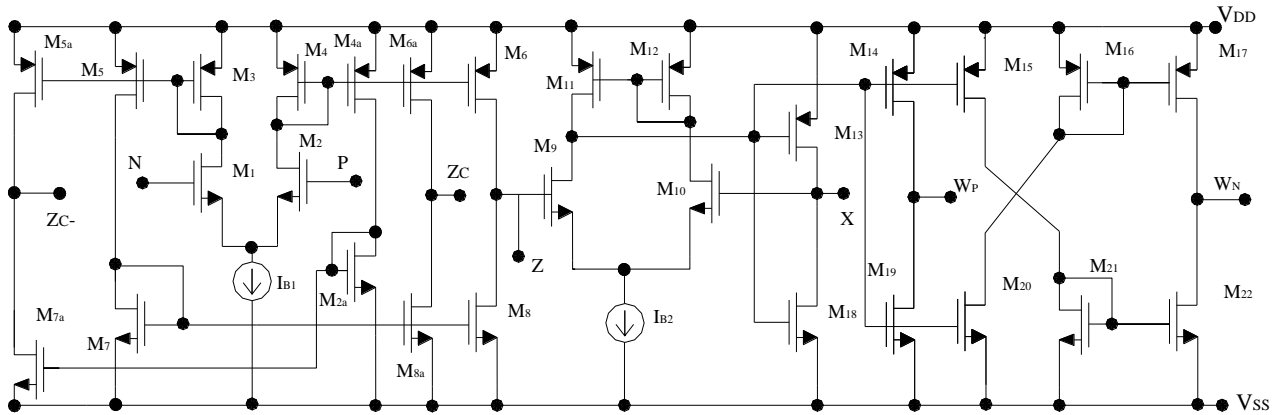


Fig. 5 CMOS realization of the voltage differencing current conveyor [23].

oscillation condition and mathematical formula to attain oscillation frequency are given by (18) and (19), respectively.

$$s^2 + s \left[\frac{1}{C_2} \left(\frac{1}{R_b} - g_3 \right) + \frac{1}{C_1 R_a} \right] + \frac{1}{C_1 C_2} \left(\frac{1}{R_a R_b} - \frac{g_3}{R_a} + \frac{g_3}{R_2} \right) = 0 \quad (17)$$

$$\text{Condition of Oscillation: } \frac{1}{C_2} \left(\frac{1}{R_b} - g_3 \right) + \frac{1}{C_1 R_a} = 0 \quad (18)$$

$$\text{Oscillation Frequency: } \omega_0'' = \sqrt{\frac{1}{C_1 C_2} \left(\frac{1}{R_a R_b} - \frac{g_3}{R_a} + \frac{g_3}{R_2} \right)} \quad (19)$$

The above equations are derived after taking into consideration the assumptions, given in (16), which was done for the purpose of simplifying the mathematical analysis. The actual values of parasitic elements, such as $R_x = 43\Omega$, $R_z = 362k\Omega$, $R_p = R_n = 141k\Omega$, $C_p = C_n = 0.92pF$, have been taken from [21]. If these values are combined, as per the circuit theory, with passive element values, i.e., $C_1 = C_2 = 35pF$, $R_1 = 3.65k\Omega$, $R_2 = 2.1k\Omega$, then frequency was obtained as 1.05MHz. Ideally, the frequency was 1.07MHz. Thus, the presence of parasitics imposes an inconsiderable effect on oscillator design, thereby making it a parasitic insensitive configuration.

5 Simulation Results

For the purpose of justifying the idea of single-resistance-controlled oscillator, it is verified through software simulations in this section. Cadence PSPICE software simulation tool has been used to obtain all the simulation results. The simulation results are bifurcated into two parts. At the outset, simulations are presented using CMOS version of the VDCC, later on simulations have been performed using the PSPICE model of commercially available integrated circuits.

5.1 Simulation Results Using CMOS Model of VDCC

The well-known CMOS version of the VDCC has been considered here, taken from [23]. The aspect ratios used for simulating the design circuit are shown in Table 2 [24]. The validation has been performed with

Table 2 Aspect ratio of MOS transistors [24].

Transistors	W/L [μm]
M1-M4	3.6/1.8
M5-M6, M4a, M5a, M6a	7.2/1.8
M7-M8, M2a, M7a, M8a	2.4/1.8
M9-M10	3.06/0.72
M11-M12	9/0.72
M13-M16	14.4/0.72
M17	13.85/0.72
M18-M22	0.72/0.72

0.18 μ m TSMC technology whose process parameters are stated in [30], with supply voltages being $V_{DD} = -V_{SS} = 0.9V$ and bias currents being $I_{B1} = 50\mu A$ and $I_{B2} = 100\mu A$. By adjusting the above specified bias current and voltage values a trans-conductance factor (g_m) of 277 $\mu A/V$ is attained.

The elementary waveform, presenting the workability of the designed sinusoidal oscillator, is transient response where exponentially growing oscillation starts and attains a stable amplitude at a fixed frequency value, shown in Fig. 6. To get this sustained and desired frequency of oscillation, the following specified passive components values are chosen, $R_1 = 3.65k\Omega$, $R_2 = 2.1k\Omega$, $C_1 = C_2 = 35pF$, and $g_m = 277\mu A/V$. The frequency attained through simulation is 1.05 MHz, though it was designed to get a value of 1.07MHz, thus producing an error of 1.87% in the simulated waveform. To see the clarity of the waveform, only a few cycles of its time period, also known as steady-state response, is represented in Fig. 7. The FFT (Fast Fourier Transform) analysis at designated frequency has also been obtained in Fig. 8, to see the sub-harmonics present in the generated signal. To widen the scope of the oscillator's generated waveforms and to ensure its stretchable range, a graph has been plotted between frequencies of oscillation with respect to the external grounded passive

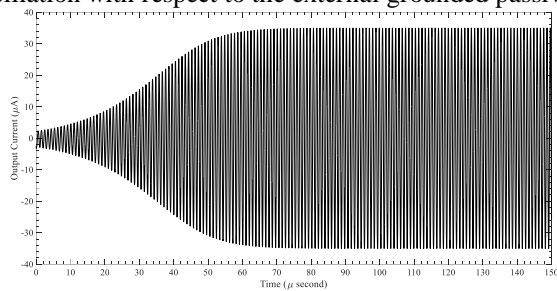


Fig. 6 Transient response of the proposed oscillator circuit.

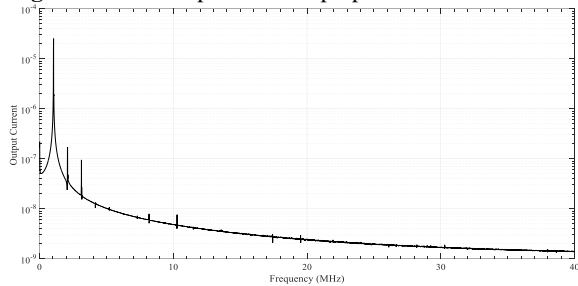


Fig. 8 FFT diagram for the designated frequency of oscillation.

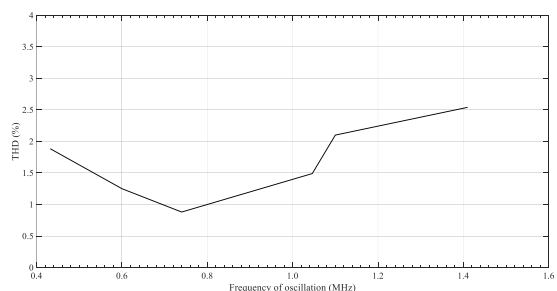


Fig. 10 Total harmonic distortion of the design oscillator at certain frequencies.

resistance R_2 , shown in Fig. 9. The percentage of distortion introduced in the circuit due to the presence of sub-harmonics, which is given in Fig. 8, has been presented in Fig. 10, for all usable frequencies.

5.2 Simulation Results Using IC version of VDCC

In this section of simulation results, the same sinusoidal oscillator circuit, but with another model of VDCC, has been tested. Here the VDCC has been designed using off-the-shelf Integrated Circuits (ICs). There are various possible solutions to realize VDCC with commercial available ICs such as (a) Utilizing AD844 and LM13700 [31] (b) possible realization using AD844 and CA3080 (not published anywhere yet) (c) employing only OPA 860 [23, 28]. The approach mentioned in the last is utilized here, due to certain advantages.

- (i) Wider bandwidth of OPA860
- (ii) Only a single variety of IC is sufficient to design complete VDCC block
- (iii) The transconductance of this special purpose amplifier can directly be controlled by an external passive resistor.

Fig. 11 shows the realization of VDCC as an active building block, employing OPA860 along with few

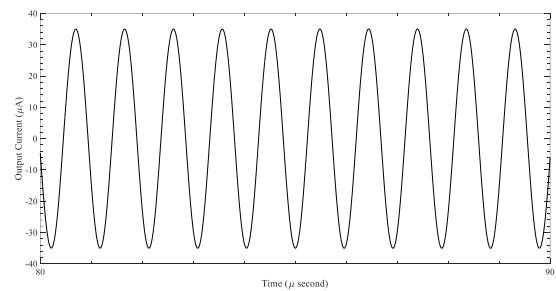


Fig. 7 Steady-state waveform of the designed oscillator.

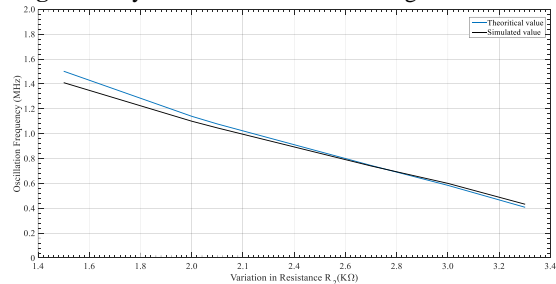


Fig. 9 Frequency of oscillation with respect to a grounded passive resistor R_2 .

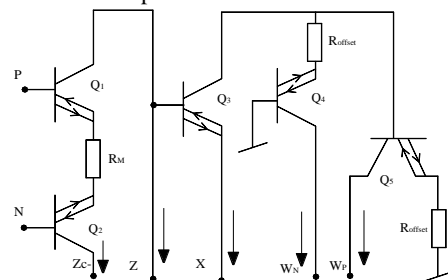


Fig. 11 Realization of VDCC utilizing discrete components [33].

passive components. Here it is worth noting that the first ever VDCC realization using OPA 860 is given in [28], later on a modified version of the same is presented in [23]. In [33] a step further modification has been performed in the circuit layout to get the improved results and the same model of VDCC has been used here for simulation purposes.

OPA860 is also known as diamond transistor or can also act as a current-controlled current conveyor (CCCII). The discrete realization of VDCC is explained as follows. Here Q1 and Q2 form the OTA part of VDCC whereas Q3, Q4, and Q5 make the output available for X, WP, and WN terminals [33].

The passive component values used here for simulation, are $R_1 = 0-300\Omega$, $R_2 = 300\Omega$, $C_1 = C_2 = 470\text{pF}$ and $R_M = 1/g_m = 330\Omega$. The theoretical frequency obtained, with the above-specified values, is 726.7kHz and the simulated frequency has been obtained as 680.7kHz, with an error of 6.7% in software simulations. The transient waveform of the proposed oscillator, when designed using OPA860, is shown in Fig. 12 whereas the steady-state response is represented in Fig. 13. FFT analysis of the derived oscillator at designated frequency is presented in Fig. 14.

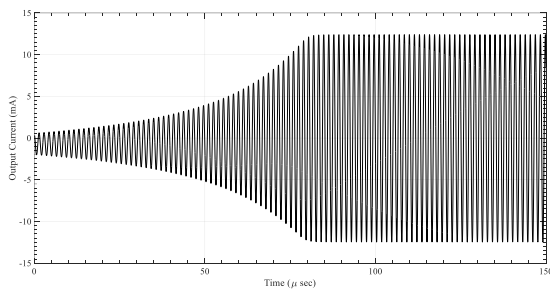


Fig. 12 Transient waveform of the proposed circuit using ICs.

6 Experimental Work

For practical verification of the designed oscillator, VDCC is realized with the help of OPA 860 IC which is an 8 pin SOIC, converted into DIP using SOIC to DIP converter. The actual hardware diagram of the derived circuit is shown in Fig. 15. The instruments used while performing the experiment are two Keysight programmable DC power supply (E3632A), Caddo 803, 30MHz 2 channel 4 trace Cathode Ray Oscilloscope (CRO), and Keysight digital multimeter (U1252B). The supply voltage requirement, to operate the experimental setup, is $\pm 5\text{V}$. In order to generate the waveform, the passive element values have been kept same as those which were used during software simulations using OPA860. Fig. 16 shows the real waveform as displayed on the screen of the oscilloscope. The wide range of operating frequency, with respect to the variation in the value of a physical resistance R_2 , is depicted in Fig. 17. This graph includes three different curves, i.e., ideal frequency values, simulated values, and experimental frequencies, obtained on varying R_2 .

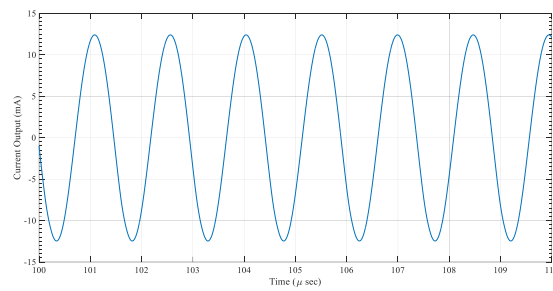


Fig. 13 Steady-state response of the oscillator using OPA860.

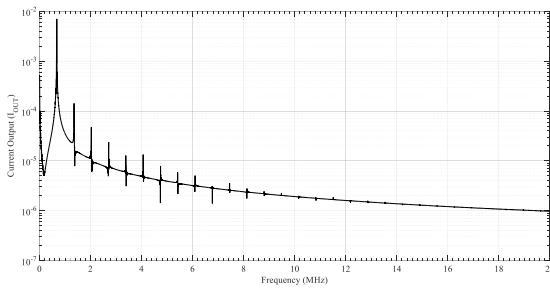


Fig. 14 FFT analysis of the designed oscillator.

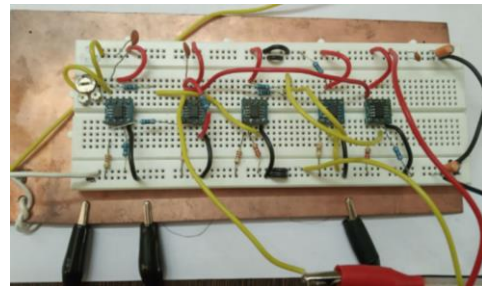


Fig. 15 Actual diagram of the oscillator using OPA860.

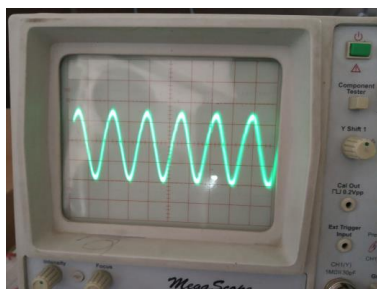


Fig. 16 Output waveform as displayed on the oscilloscope.

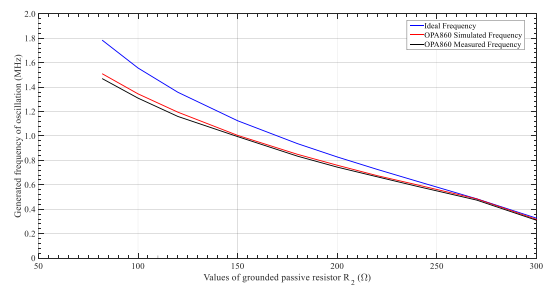


Fig. 17 Frequency of oscillation with respect to a grounded passive resistor R_2 (for OPA860).

7 Conclusion

A single-resistance-controlled oscillator using only grounded passive elements and a single active device was presented in this manuscript. The circuit is a desirable choice for integrated circuit implementation because of the utilization of all grounded passive components. Availability of output from high impedance port, negligible effect of device parasitic on design, and independent tunability of the frequency of oscillation are some of the salient characteristics of the designed circuit. All sorts of mathematical analysis, supporting the novel architecture of the circuit, are discussed in detail in the manuscript. To check the practicality of the design, both software simulation and hardware implementation results, have been included.

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