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Research Paper

A Coupled Inductor Based High Voltage Gain DC-DC Converter Using Interleaved Voltage Multiplier Cells

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Abstract: In this work, a non-isolated high step up DC-DC converter using coupled inductor and voltage multiplier cell is proposed. The proposed converter conversion ratio is efficiently extended by using a coupled inductor. An interleaved configuration of two diode-capacitor cells is applied to step up the voltage conversion ratio and decrease the voltage stress across the switches. Also, in the suggested converter high voltage gain is provided by low turn ratio of the coupled inductor which decreases the volume of cores. Moreover, the reverse recovery problem of output diode is diminished by recycling the leakage inductance energy of the coupled inductor. It causes to increase the overall system efficiency. Furthermore, the voltage multiplier cells lead to clamp the voltage spikes through the switch, when the switch turns off. The comparison between the suggested converter and similar converters is provided to verify its advantages. To validate the effectiveness of the suggested converter, a 200W laboratory prototype with 20V input and 150V output voltages operating at 25kHz switching frequency is carried out and experimental test consequences are given.

Keywords: Non-Isolated Converter, High Conversion Ratio, Coupled Inductor, Voltage Multiplier Cell.

1 Introduction

PHOTOVOLTAIC (PV) is one of the best techniques for absorbing green energy to solve the serious problems of global warming and lack of energy that occurs by energy consumption [1-3]. Also, PV is one of the most significant systems for receiving energy in the world and it will have the largest share of electricity generation among all renewable energy candidates until 2040 [4]. But there are some drawbacks in terms of PV systems as follow [5, 6]:

- The magnitude of produced voltage by PV panels is low and is changed by ambient temperature and solar radiation;
- The capability of the used converter to track the maximum power point is complex;
- The efficiency of PV modules is low.

Therefore, DC-DC converters with high conversion ratio are needed to convert the PV generated low voltage to the required high voltage level [7]. The conventional boost and buck-boost converters are famous topologies to step up the voltage. High voltage gain cannot obtain for these topologies due to losses caused by the inductor, filtering capacitor, switch and output diode. But then, the extreme increase in duty ratio of switch, makes the reverse recovery problem appear seriously and also, the power rating of the diode is increased [8-11]. The quadratic boost structure, which utilizes a single power switch, is another converter to step up the voltage, where the conversion ratio is specified as a quadratic function of the duty ratio [12, 13]. However, excessively increasing of duty cycle in these topologies restricts the switching frequency and system size. So, under this condition, the output voltage is very low and the problem of electromagnetic

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interference (EMI) is intensified [14]. However, a lot of active switches are necessary to realize a high voltage gain. Also, the control unit is complicated, which causes the complexity of the power circuit and also cost increasing [15]. A coupled inductor is modeled as a transformer function to increase the voltage conversion ratio in non-isolated DC-DC converters [16-19]. The main drawback in terms of these converters is voltage spikes through the active switches due to the leakage inductance and high costs. In order to solve these problems, the clamped circuits are utilized which can provide zero voltage operation of switches (ZVS) and zero current operation of switches (ZCS) conditions, which results in complexity of power circuit and its high cost [20-22]. Various high gain DC-DC structures based on the coupled inductor and switch capacitor structure have been introduced in the literature [23, 24]. The main features of these converters are that the voltage conversion ratio can be regulated in PWM mode; less active power switches and magnetic components are utilized. In order to achieve high voltage gain, the switched capacitor units and the boost converter can be combined [25-27]. These converters can obtain appropriate voltage gain with low current ripple contents which leads to reduce the EMI. The basic impediment of these topologies is high current and voltage ripples [27]. Interleaved converters with small size, weight and a small amount of magnetics are used in high power applications. Therefore, the sizes of input inductors and capacitors are intensely reduced. The voltage stress through the power switches is not higher than the half of the produced voltage for a single multiplier stage. However, reverse recovery currents through the multiplier diodes are large [28].

In this study, a novel non-isolated DC-DC converter with high conversion ratio is proposed. The suggested structure consists of a coupled inductor with two windings, just one active switch and two interleaved voltage multiplier units that are composed of diodes and capacitors. The voltage gain of the presented converter depends on the turn's ratio of the coupled inductor. The produced leakage inductance energy by coupled inductor is retrieved which leads to improving the overall efficiency of the converter. The diode-capacitor units are utilized to increase the output voltage and also, clamp the voltage through the switch which leads to reduce the voltage stress of the semiconductors. Thus, by using single switch with lower resistance $R_{DS\,(on)}$, the conduction losses are reduced.

2 Operational Function of Proposed DC-DC Converter

Fig. 1 illustrates the power circuit and equivalent circuit of the suggested topology. As shown in this figure, the proposed structure includes single active switch, an input inductor L_{in} for reduction of input current ripple, a coupled inductor contains inductors L_{t1} and L_{t2} with n=2, the first voltage multiplier cell contains two capacitors C_2 and C_3, and diodes D_1 and D_2, and second voltage multiplier cell contains capacitor C_1 and diode D_o. Capacitor C_3 and diode D_1 act as a clamp circuit to decrease the peak voltage of the switch. The coupled inductor's primary and secondary inductors are denoted via L_{t1} and L_{t2}. An ideal transformer with turn ratio of n (n_1/n_2) is used for modeling the coupled inductor where L_k is leakage inductance and L_m is magnetizing inductance.

To ease the analysis of the presented converter, the following suppositions are considered:

- All capacitors have large contents as their voltages are fixed during one switching period.
- Input current (i_{Lin}) is continuous because of large input inductance.
- The used elements are ideal except the leakage inductance of the coupled inductor.

The proposed converter operation in CCM (Continuous Condition Mode) and DCM (Discontinuous Conduction Mode) are analyzed as given in the following. In order to facilitate the analysis, the leakage inductor of the coupled inductor (L_k), is ignored during the CCM and DCM operations.

2.1 CCM Operation

The basic waveforms of the converter operation in CCM are illustrated in Fig. 2(a). Two time intervals can be considered for each switching period in CCM operation.

First Mode: At this time instant, the switch S starts to conduct. Diodes D_1 and D_o are in reverse bias by voltages V_{C3} and V_o-V_{C3}, respectively. The only diode

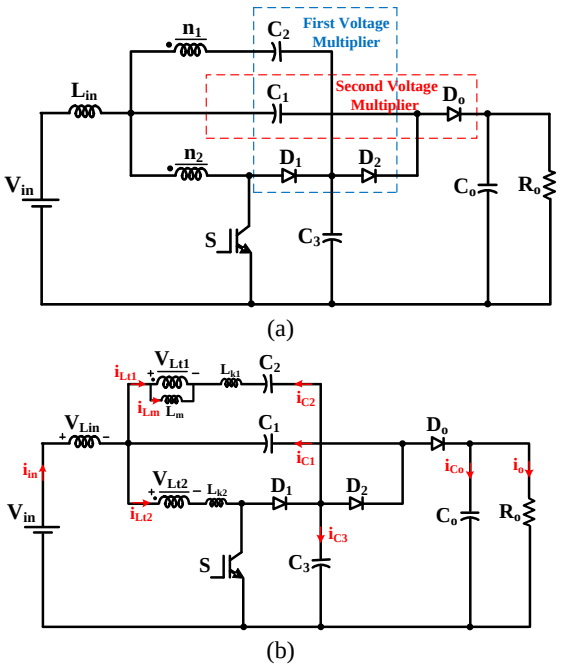


Fig. 1 Equivalent circuits of suggested converter: a) power circuit, and b) equivalent model.

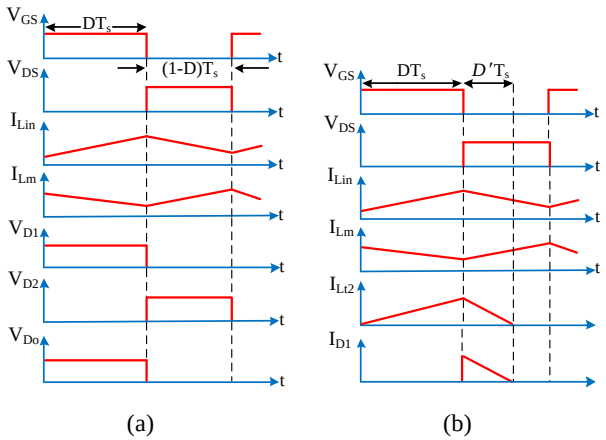


Fig. 2 Basic waveforms of the suggested converter: a) CCM operation, and b) DCM operation.

D_2 is conducting in this mode. DC energy from input source is transferred to the input inductor and the coupled inductor's secondary side. It increases currents i_{Lin} and i_{Lt2} linearly and both inductances are charged. In this mode, capacitors C_2 and C_3 are discharged and clamp through the voltage of capacitor C_1 and secondary side of the coupled inductor, L_{t2}. Therefore, the capacitor C_1 voltage can be increased by the stored energy in the coupled inductor. The current track of the first mode is depicted in Fig. 3(a).

Second Mode: In this time instant, the power switch is switched off. At this time, diodes D_1 and D_o start to conduct and diode D_2 is blocked by voltage V_o-V_{C3}. The stored energy in inductor L_{in} is transferred to the magnetizing inductance of coupled inductor (L_m), and input inductance is discharged. It increases current i_{Lm} linearly. Also, the stored energy in inductor L_{t2} charges capacitors C_2 and C_3. In this mode, the energy required for the load is provided from the input voltage V_{in}, input inductor and the stored energy in capacitor C_1 which increases the output voltage. The current track of this mode is depicted in Fig. 3(b).

2.2 DCM operation

Converter operation in DCM is divided in three switching modes. Fig. 2(b) illustrates the basic waveforms of voltage and current of the converter operation in DCM. Modes 1 and 2 are similar to modes 1 and 2 in CCM operations, which are depicted in Figs. 3(a) and 3(b), respectively. Mode 3 is occurred when the energy of the secondary side of the coupled inductor (L_{t2}), is completely depleted. In this time interval, the active switch is still OFF and diodes D_1 and D_2 are reverse biased by voltages V_{C3}-V_{SW} and V_o-V_{C3}, respectively. Only diode D_o conducts in this time interval. During this switching time, the current which flows in the secondary side of the coupled inductor (i_{Lt2}), decrease to zero. The load required energy is provided from output capacitor C_o, DC source, input

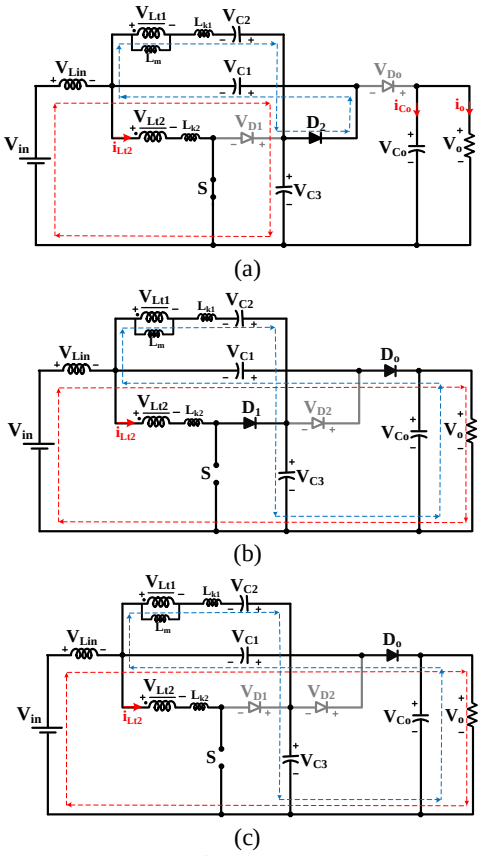


Fig. 3 The current track of operation modes during switching time: a) switch is on, b) switch is off, and c) DCM operation.

inductor, and capacitor C_1. Fig. 3(c) illustrates the current track of the third Mode in DCM operation.

3 Steady-State Analysis of Suggested Converter

This section provides the steady-state analysis of the suggested converter operation. In order to have a simple analysis, all converter elements are assumed to be ideal. In addition, the leakage inductance is ignored in analysis of the coupled inductor because of its small value. The converter operation is studied in all CCM, DCM, and BCM (Boundary Conduction Mode) conditions.

3.1 CCM Operation

Two different modes are considered for the converter operation in CCM. The equations related to Fig. 3(a), can be written as follows.

$$V_{Lin} = V_{in} + V_{C1} - V_{C3} \quad (1)$$

The voltages across inductors L_{t1} and L_{t2} are calculated as given in (2) and (3).

$$V_{Lt1} = V_{C2} - V_{C1} \quad (2)$$

$$V_{Lt2} = V_{C3} - V_{C1} \quad (3)$$

As shown in Fig. 3(b), the switch S is switched off in

second mode and above equations can be rewritten.

$$V_{Lin} = V_{c1} + V_{in} - V_o \quad (4)$$

$$V_{Lt1} = V_o + V_{C2} - V_{C1} - V_{C3} \quad (5)$$

$$V_{Lt2} = V_o - V_{C1} - V_{C3} \quad (6)$$

Volt-second balance law is utilized for the inductors L_{in}, L_{t1}, and L_{t2} as follows:

$$\int_0^{DT_s} V_{Lt1(on)} dt + \int_{DT_s}^{T_s} V_{Lt1(off)} dt = 0 \quad (7)$$

$$\int_0^{DT_s} V_{Lin(on)} dt + \int_{DT_s}^{T_s} V_{Lin(off)} dt = 0 \quad (8)$$

$$\int_0^{DT_s} V_{Lt2(on)} dt + \int_{DT_s}^{T_s} V_{Lt2(off)} dt = 0 \quad (9)$$

From (1)-(9), the voltages of the capacitors C_1, C_2, and C_3 can be obtained as follows:

$$V_{C1} = \frac{V_o (D-1)^2 + V_{in}(2D-1)}{1-D} = \frac{n-D}{2n-1} V_O \quad (10)$$

$$V_{C2} = \frac{D}{1-D} V_{in} = \frac{D(n-1)}{2n-1} V_o \quad (11)$$

$$V_{C3} = \frac{V_{in}}{1-D} = \frac{(n-1)}{2n-1} V_o \quad (12)$$

The voltage gain in CCM operation (M_{CCM}), is obtained as follows:

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2n-1}{(n-1)(1-D)} \quad (13)$$

With regard to Fig. 3(a), the peak voltage of the main switch (V_{Sw}), is determined as follows:

$$V_{SW} = V_{C3} = \frac{n-1}{2n-1} V_o \quad (14)$$

Also, the voltage across diodes (V_{D1}, V_{D2}, and V_{Do}) are calculated as follows:

$$V_{D1} = V_{SW} = \frac{n-1}{2n-1} V_o \quad (15)$$

$$V_{D2} = V_{Do} = \frac{n}{2n-1} V_o \quad (16)$$

3.2 DCM Operation

There are three time intervals in DCM operation. Modes 1 and 2 in DCM are similar to the modes 1 and 2 in CCM. Fig. 3(c) illustrates the mode 3 in DCM operation. In this mode, only diode D_o conducts and so, the following equations are derived:

$$V_{Lt1} = V_o - V_{C1} + V_{C2} - V_{C3} \quad (17)$$

$$V_{Lt2} = 0 \quad (18)$$

$$V_{Lin} = V_{c1} + V_{in} - V_o \quad (19)$$

Volt-second law is used for the coupled inductors and the following equations are achieved:

$$\int_0^{DT_s} V_{Lt1}^{(1)} dt + \int_{DT_s}^{(D+D')T_s} V_{Lt1}^{(2)} dt + \int_{(D+D')T_s}^{T_s} V_{Lt1}^{(3)} dt = 0 \quad (20)$$

$$\int_0^{DT_s} V_{Lt2}^{(1)} dt + \int_{DT_s}^{(D+D')T_s} V_{Lt2}^{(2)} dt + \int_{(D+D')T_s}^{T_s} V_{Lt2}^{(3)} dt = 0 \quad (21)$$

$$\int_0^{DT_s} V_{Lin}^{(1)} dt + \int_{DT_s}^{(D+D')T_s} V_{Lin}^{(2)} dt + \int_{(D+D')T_s}^{T_s} V_{Lin}^{(3)} dt = 0 \quad (22)$$

Therefore, the voltage across the capacitors C_1, C_2, and C_3 can be determined in the following.

$$V_{C1} = \frac{(D^2 + nD' - D)V_o}{D(D-1) + D'(D+2n-1)} \quad (23)$$

$$V_{C2} = \frac{D(nD' + D - 1)V_o}{D(D-1) + D'(D+2n-1)} \quad (24)$$

$$V_{C3} = \frac{D(D-1) + D'(2D-1)}{D(D-1) + D'(D+2n-1)} V_o \quad (25)$$

D' and the voltage gain of the suggested converter during this time interval are calculated as given in (26) and (27).

$$D' = \frac{D(1-D)V_{in}}{V_{in}(D+2n-1) - V_o(n-1)(1-D)} \quad (26)$$

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{D'(D+2n-1) + D(D-1)}{D'(n-1)(1-D)} \quad (27)$$

The peak current value through the secondary side inductor of the coupled inductor (I_{L2}), is equal to:

$$I_{Lt2} = \frac{(1-D)DT_s}{(1-2n)L} V_o \quad (28)$$

By knowing that in steady-state operation, the average currents through the capacitors are zero, the average current of diodes D_1, D_2, and D_o are equal to the average of output current (I_o), so we have:

$$I_{D1} = I_{D2} = I_{Do} = I_o = \frac{1}{2} D' I_{L2} \quad (29)$$

Substituting (28) and (29) into (26), the voltage conversion ratio of the converter in DCM is achieved as follows:

$$M_{DCM} = \frac{D+2n-1}{(n-1)(1-D)} - \frac{D}{n-1}\sqrt{\frac{D}{2k_{crit}(2n-1)}} \quad (30)$$

3.3 BCM Operation

Since the voltage conversion ratio in CCM operation is equal to the voltage gain in DCM operation, it means that the converter operates in BCM. Based on (13) and (27), the normalized time constant of boundary operation is represented by the following equations.

$$M_{CCM} = M_{DCM} \tag{31}$$

$$\tau_{L2(crit)} = \frac{D(1-D)^2}{2(2n-1)} \tag{32}$$

Fig. 4 illustrates the curve of boundary normalized secondary winding of the coupled inductor time constant $\tau_{L2(cirt)}$ versus duty ratio (D). The suggested converter operates in the CCM when $\tau_{L2(cirt)}$ is higher than τ_{L2}. Conversely, the converter operates in DCM when τ_{L2} is determined to be higher than $\tau_{L2(cirt)}$.

3.4 Current Analysis

In the first time interval, when the active switch is switched on, the capacitor currents are represented as follows:

$$I_{C1(ON)} = I_{Lt1} + I_{Lt2} - I_{in} \tag{33}$$

$$I_{C2(ON)} = -I_{Lt1} \tag{34}$$

$$I_{C3(ON)} = I_{C1(ON)} - I_{C2(ON)} \tag{35}$$

$$I_{CO(ON)} = -I_O \tag{36}$$

When the switch is turned off in the second time interval, the following equations are achieved for the capacitors current:

$$I_{C1(OFF)} = I_{Lt1} + I_{Lt2} - I_{in} \tag{37}$$

$$I_{C2(OFF)} = -I_{Lt1} \tag{38}$$

$$I_{C3(OFF)} = I_{D1} - I_{C2(OFF)} \tag{39}$$

$$I_{CO(OFF)} = -I_{C1(OFF)} - I_o \tag{40}$$

By utilizing the current-second balance law for capacitors, the average current through the capacitors in the first and the second modes are achieved in the following:

$$I_{C1,ON} = -I_{C2,ON} = I_{C3,ON} = \frac{I_{out}}{D} \tag{41}$$

$$I_{C2,OFF} = -I_{C1,OFF} = -I_{C3,OFF} = \frac{I_{out}}{1-D} \tag{42}$$

Now, by remarking n=2, the following equations are obtained:

$$I_{Lt1} = I_{C2,ON} = \frac{I_o}{D} \tag{43}$$

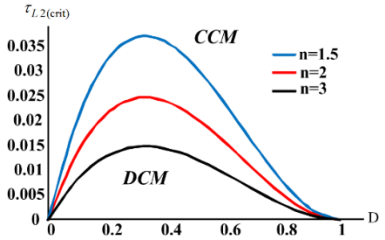


Fig. 4 Normalized inductor time constant of boundary operation.

$$I_{Lt2} = I_{C1,ON} + I_{C2,ON} + I_{in} = \frac{3I_o}{1-D} \tag{44}$$

$$I_{SW} = I_{Lt2} = \frac{3I_o}{1-D} \tag{45}$$

$$I_{D1} = I_{Lt2} = \frac{3I_o}{1-D} \tag{46}$$

$$I_{D2} = I_{C1,ON} = \frac{I_o}{D} \tag{47}$$

$$I_{Do} = -I_{C1,OFF} = \frac{I_o}{1-D} \tag{48}$$

4 Key Parameters Design Procedure

4.1 Input Inductor

The converter input current ripple should be low as possible as, to increase the lifespan of energy sources connected to the converter. Therefore, input inductor (L_{in}) is designed to have an input current ripple value nearly 10-20% of the average input current, which can be obtained as given in (49).

$$L_{in} = \frac{nV_{in}D}{(2n-1)f_s\Delta I_{Lin}} \tag{49}$$

4.2 Magnetizing Inductor and Turn Ratio of Coupled Inductor

Coupling inductive value is determined by magnetic inductance (L_m). It is important to design the magnetizing inductance as the converter works in CCM. So, the acceptable magnetizing inductor value is obtained as given in the following:

$$L_m = \frac{nV_{in}D}{f_s\Delta I_{Lm}} \tag{50}$$

where ΔI_{Lm} is the current ripple of the magnetizing inductor. The turn ratio should be selected in such a way that the voltage rating of devices be low. To obtain the turn ratio of the coupled inductor, the following equation is used:

$$n = \frac{n_1}{n_2} = \frac{V_o(1-D) - V_{in}}{V_o(1-D) - 2V_{in}} \tag{51}$$

The turn ratio of the coupled inductor is estimating by selecting the switching duty ratio, and also the power device voltage and current stresses can be determined.

4.3 Capacitors

The capacity of the output capacitor, C_o, which limits the output voltage in CCM operation, can be written as follows:

$$C_o = \frac{P_o D}{f_s V_o \Delta V_o} \tag{52}$$

According to the capacitor currents, the capacity of the capacitors C_1, C_2, and C_3 is given as follows:

$$C_{1,2,3} = \frac{P_o}{f_s V_o \Delta V_{C1,2,3}} \quad (53)$$

ΔV is named as capacitor voltage ripple which is considered 5-10% of average voltage. The voltage and current waveform of capacitors are depicted in Fig. 5.

4.4 System Losses Analysis

The power losses of the suggested converter can be divided into the following groups:

1. Power losses of the switch;
2. Power losses of the diodes;
3. Power losses of the Capacitors;
4. Power losses of the magnetic components.

Some variable symbols of parasitic elements are introduced in the following.

$r_{DS\text{-}ON}$: resistance of power switch in On-state;
r_C: ESR values of Capacitors;
r_D: On-state resistance of diodes D_o, D_1, D_2;
v_{FD}: Diodes forward voltages;
r_L: The ESR value of the magnetic components.

The power losses of the power switch can be determined by summation of the conduction and switching losses. The conduction loss of the active switch, P_{rDS}, is achieved in the following.

$$P_{rDS} = r_{DS} I_{S,rms}^2 \quad (54)$$

Switching loss is occurs when the active switch is switched ON and OFF. So, the converter switching loss (P_{SW}), is written as follows:

$$P_{SW} = \frac{1}{2} f_s (t_r + t_d) I_{sw} V_{sw} \quad (55)$$

where f_s is switching frequency, V_{sw} is the average voltage through the switch, I_{sw} is the average current through the switch, t_r is the rise time of the switch and t_d is the turn-off delay time. Therefore, the total power loss of the switch (P_{switch}) is obtained as given in (56).

$$P_{switch} = P_{rDS} + P_{SW} \quad (56)$$

The major loss of a diode is conduction loss due to the existence of the internal resistance, and diode forwards voltage loss. The conduction losses through the Diodes are computed as follows:

$$P_{rf} = r_{Diodes} I_{rms,Diodes}^2 \quad (57)$$

and diodes forward voltage losses are obtained as follows:

$$P_{vF(D_{Diodes})} = V_{F(Diodes)} I_{(avg)Diodes} \quad (58)$$

Power losses of capacitors due to ESR are determined as given in (58).

$$P_{rC(Capacitors)} = r_{Capacitors} I_{Capacitors,rms}^2 \quad (59)$$

The magnetic losses due to the existence of the coupled inductor and input inductor, are calculated in the following.

$$P_{rL} = r_L I_{L,rms}^2 \quad (60)$$

By highlighting the overall system losses, the following equation is utilized to estimate the efficiency of the suggested converter:

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} \times 100\% \quad (61)$$

All mentioned losses by considering n=2, D=0.6 and related to the experimental results in the nominal output power, are shown in Fig. 6. It should be noted that the core losses through the input inductor and coupled inductor are negligible by comparing to other conduction losses. Thus, in the efficiency calculation, the core losses are not considered.

4.5 Dynamic Response Analysis

The dynamic proficiency of the proposed structure is studied using the state-space average method. The system equations are provided as state, input and control

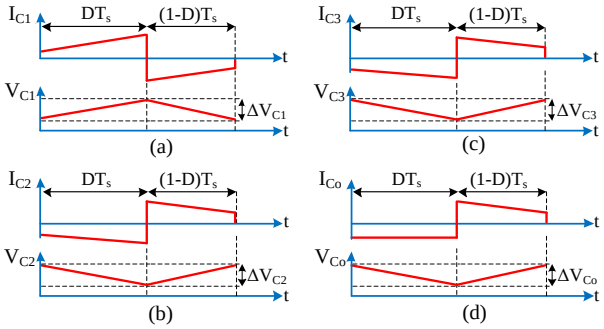


Fig. 5 Voltage and current waveforms of capacitors: a) C_1, b) C_2, c) C_3, and d) C_o.

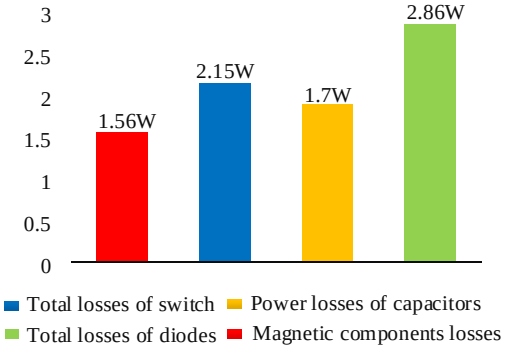


Fig. 6 Components power losses at full load.

variable functions which are shown in the state-space form as follows.

$$\begin{aligned} \hat{x}_i'(t) &= A\hat{x}_i(t) + B\hat{u}_i(t) \\ \hat{y}_i(t) &= C\hat{x}_i(t) + D\hat{u}_i(t) \end{aligned} \tag{62}$$

The following presumptions are investigated in order to have a state equation,

- All components are considered ideal;
- The input current is continuous.

In the analysis, $\hat{x}_i'(t)$ is the vector of state variables, $\hat{u}_i(t)$ is the vector of input variables, and $\hat{y}_i(t)$ is the vector of output variables which are defined as follow:

$$\hat{x} = [\hat{i}_{Lin}, \hat{i}_{Lk1}, \hat{i}_{Lk2}, \hat{v}_{C1}, \hat{v}_{C2}, \hat{v}_{C3}, \hat{v}_{Co}] \tag{63}$$

$$\hat{u} = [\hat{v}_{in}, \hat{i}_o, \hat{i}_{D1}, \hat{d}] \tag{64}$$

$$\hat{y} = [\hat{i}_{in}, \hat{v}_o] \tag{65}$$

By utilizing Kirchhoff's voltage and current laws for each mode of operations, the associated matrixes related to equation (62), is obtained:

$$A = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_{in}} & 0 & -\frac{D}{L_{in}} & \frac{D-1}{L_{in}} \\ 0 & 0 & 0 & -\frac{1}{L_{k1}} & \frac{1}{L_{k1}} & \frac{D-1}{L_{k1}} & \frac{1-D}{L_{k1}} \\ 0 & 0 & 0 & \frac{-1}{L_{K2}} & 0 & \frac{2D-1}{L_{K2}} & \frac{1+D}{L_{K2}} \\ -\frac{1}{C_1} & \frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{D}{C_2} & 0 & 0 & 0 & 0 & 0 \\ \frac{1-2D}{C_3} & \frac{1+3D}{C_3} & \frac{1+2D}{C_3} & 0 & 0 & 0 & 0 \\ 0 & \frac{1-D}{C_o} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{66}$$

$$B = \begin{bmatrix} \frac{1}{L_{in}} & 0 & 0 & \frac{V_o - V_{C3}}{L_{in}} \\ 0 & 0 & 0 & \frac{V_{C3} - V_o}{L_{k1}} \\ 0 & 0 & 0 & \frac{2V_{C3} - V_o}{L_{k2}} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{I_{Lk1}}{C_2} \\ 0 & 0 & \frac{1-D}{C_3} & \frac{3I_{Lk1} + I_{Lk2} - I_{Lin} - I_{D1}}{C_3} \\ 0 & \frac{-1}{C_o} & 0 & 0 \end{bmatrix} \tag{67}$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{68}$$

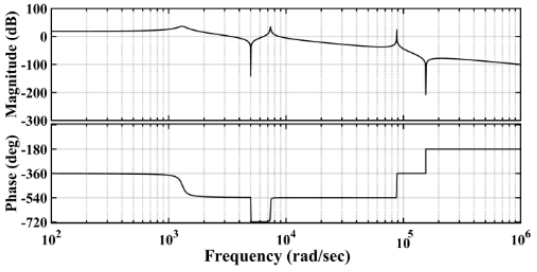
The dynamic analysis of the proposed converter based on open-loop transfer function has been performed using the Bode diagram. The element values are determined as follows: $L_{k1}=L_{k2}=2\mu$H, L_{in}=1.5mH, $C_1=C_2=C_3$=200μF, C_o=1500μF, D=0.6 and n=2. The Bode diagram of the open-loop transfer function in the Laplace domain is depicted in Fig. 7. Regarding Fig. 7(a), the control loop can be designed for the suggested converter as depicted in Fig. 7(b).

5 Comparison Study

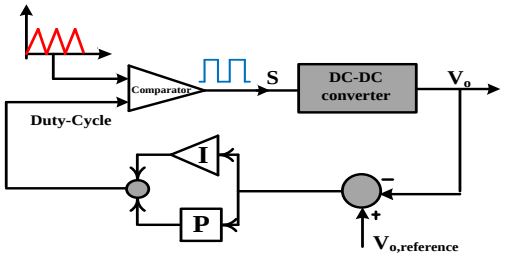
In this portion, the proposed DC-DC converter is compared with some similar topologies. Comparison results are given in Table 1.

By considering the voltage gain item, it is clear that when the value of n is closer to 1, it leads to achieving the higher voltage gain. In addition, it causes to reduce the normalized voltage stress through the power components. Conventionally, n has to be large to achieve a high conversion ratio, however, by increasing the value of n excessively, converter volume and cost will be increased. By considering the voltage gain equation of the suggested converter, it is clear that the high voltage conversion ratio is achieved for low value of n which leads to decrease in the core volume. Also, the efficiency of the proposed structure is compared with the other works at the same power.

Fig. 8(a) illustrates the voltage gain versus duty ratio for the proposed topology and the other converters. In this comparison, the coupled inductor turn ratio in all of the converters is equal to 2. The presented converters in [16] and [17] have high voltage rate, but they require an additional high rating switch which increases the cost of the converter. The converter proposed in [18] has high output voltage and high voltage stress through the switch. Also, the efficiency of the converter presented in [18] is too low for high voltage gain applications. Although, the structure introduced in [26] has a higher voltage gain in large duty cycles, but the peak voltage



(a)



(b)

Fig. 7 a) Open-loop transfer function of the suggested structure, and b) Control loop of the suggested structure.

through the switch increases exponentially.

Related to the presented converter voltage gain equation, it can be noticed that by choosing the suitable turn ratio for the coupled inductor, a high voltage gain can be provided. Fig. 8(b) illustrates comparison results of the voltage stress through the active switch between the proposed structure and the other topologies. As shown in this figure, the voltage across the switch of the suggested converter is reduced when $n > 1$ and it is nearly equal to 1. Also, it can be concluded that the peak voltage of switch in the proposed topology is reduced by decreasing the turn ratio (turn ratio should be larger than 1). Indeed, the voltage gain and the peak voltage through the switch in the suggested converter have been improved by comparing the other converters. Therefore, $R_{DS\text{-}ON}$ is decreased for the proposed converter and also, the efficiency is increased. By considering the comparison results, it has to be mentioned that the presented converter is a better choice for renewable energy systems.

6 Experimental Test Result

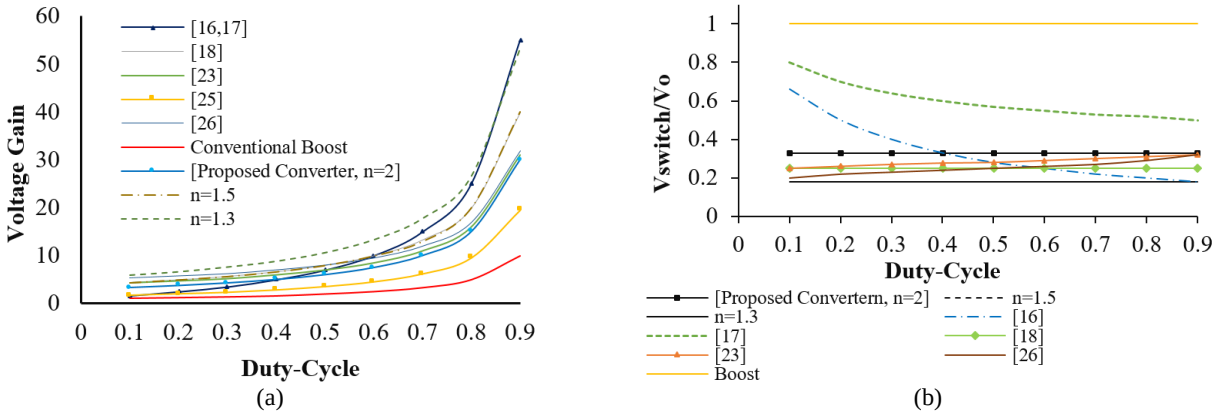
For investigating the theoretical analysis, the topology of the suggested converter has been constructed and tested in the laboratory. For the practical implementation of the converter, a microcontroller is required to control and generate the switching signals. In this work, microcontroller ATMEGA16 has been used. The experimental prototype is shown in Fig. 9 which contains power circuit and control unit. The characteristic of the prototype components is shown in Table 2.

The basic experimental results waveforms of the converter operation in CCM are illustrated in Figs. 10-12. The voltage stress and gate driving waveforms of

Table 1 Comparison results of the proposed DC-DC converter with some of the previous converters.

Converter	Voltage gain	Voltage across on switch [V]	Voltage across on diodes [V]	Efficiency [%]	Number of components				
					S*	D*	C*	CL*	I*
[16]	$\frac{1+(2n+1)D}{1-D}$	$\frac{V_o}{1+(1+2n)\,D}$	$\frac{(2n+1)\,V_o}{1+(1+2n)\,D}$	95.1	2	2	2	1	1
[17]	$\frac{1+(2n+1)D}{1-D}$	$\frac{(1+nD)V_o}{1+D(2n+1)}$	$\frac{(1+n)V_o}{1+D(2n+1)}$	95	2	2	3	2	0
[18]	$\frac{n+2}{1-D}$	$\frac{V_o}{N+2}$	$\frac{n+1}{n+2}V_o$	92.5	1	3	3	1	0
[23]	$\frac{2+n-D}{1-D}$	$\frac{1}{2+n-D}V_o$	$\frac{1+nD}{2+n-D}V_o$	93.6	1	2	2	1	0
[25]	$\frac{3+D}{2(1-D)}$	$\frac{2V_o}{3+D}$	$\frac{2V_o}{3+D}$	92.2	1	4	4	0	2
[26]	$\frac{1+n(2-D)}{1-D}$	$\frac{1}{1+n(2-D)}V_o$	$\frac{1+n}{1+n(2-D)}V_o$	95	2	3	4	1	0
Conventional boost	$\frac{1}{1-D}$	V_o	V_o	-	1	1	1	0	1
Proposed	$\frac{2n-1}{(n-1)(1-D)}$	$\frac{n-1}{2n-1}V_o$	$\frac{n-1}{2n-1}V_o$	95.2	1	3	4	1	1

*S=switch, D=diodes, C=capacitors, CL=coupled inductor, I=inductor



(a) (b)

Fig. 1 Comparison results of the presented converter and some similar structures: a) voltage gain in CCM operation, and b) voltage stress through the switch.

the power switch are given in Figs. 10(a) and 10(b), respectively. As depicted in Fig. 10(b), the peak voltage through the main switch is about 49V which is too less than the output voltage. This advantage of the proposed converter allows utilizing a switch with low $R_{DS\text{-}ON}$ to reduce the conduction loss. The input current waveform is shown in Fig. 11(a). It is obvious that the ripple of the input current is close to 0.6A and the percent of current ripple is about 6%. It is clear that the input current is continuous. The voltage waveforms of the high power diodes D_1, D_2, and D_o are illustrated in Figs. 11(b)-(d), respectively. The peak voltage through diode D_1 is about 49V which is shown in Fig. 11(b). The maximum voltage across diode D_2 is approximately 94V which is shown in Fig. 11(c). Also, the voltage stress of diode D_o is about 94V which is illustrated in Fig. 11(d). It is clear that the voltage stress of the diodes is less than that of the other converters which leads to reduce conduction loss. The output voltage waveform and the measured voltage through the capacitors are illustrated in Figs. 12(a)-(d), respectively. Fig 12(a) shows the voltage waveform of the capacitor C_1 which is about 66V. The voltage waveform of the capacitor C_2 is given in Fig. 12(b) which is approximately equal to 29V. As depicted in Fig. 12(c), the voltage through the capacitor C_3 is about 49V. The input voltage is 20V, as shown in Fig. 12(d), the output voltage is boosted to almost145V. It has to be mentioned that the output voltage ripple is low and close to zero.

Table 2 Prototype converter components.

Output power (P_o)	170 W
Input voltage (V_{in})	20 V
Output voltage (V_o)	143 V
Switching frequency (f_s)	25 kHz
Turn ratio of coupled inductor $n(n_1/n_2)$	2/1
Magnetizing inductor (L_m)	196 µH
Input inductor (L_{in})	1.5 mH
Power switch (Q)	IRFP260N
Diodes (D_1, D_2, D_o)	MUR1520
Capacitors (C_1, C_2, C_3)	200 µF/220 V
Capacitor (C_o)	1500 µF/450 V

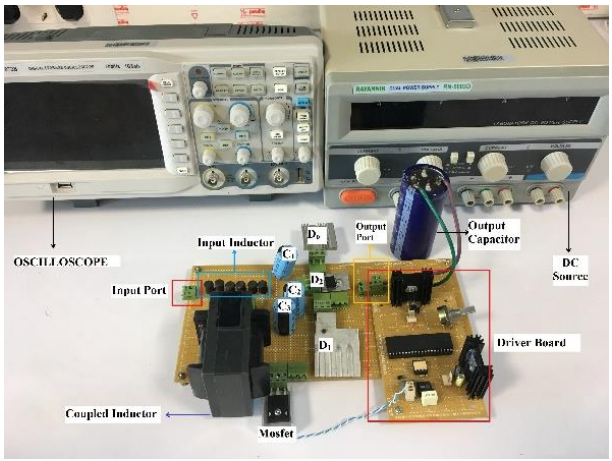
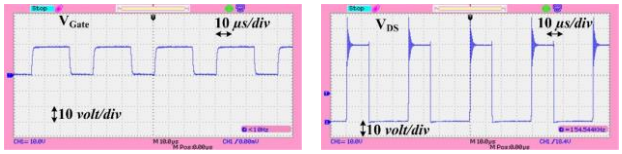


Fig. 9 Experimental prototype of the presented converter.

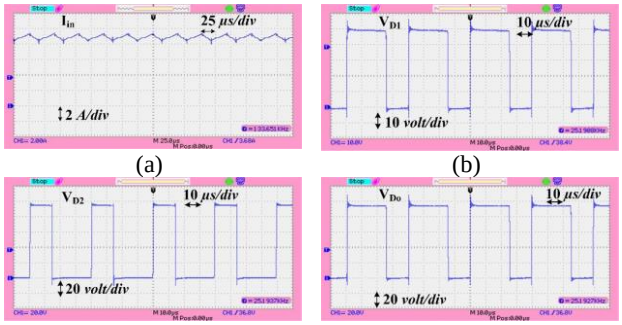
Theoretical analysis and experimental measurement results confirm that the suggested converter would be an appropriate choice for renewable energy systems such as PV due to its low input current ripple and high voltage gain. Because of the less number of power switch, lower peak voltage through semiconductors and the higher output voltage, the presented converter can be used for various power levels.

Converter measured efficiency based on output power is illustrated in Fig. 13. The used parameters in calculating the efficiency are n=2, D=0.6, f_s=25kHz. The maximum efficiency of the suggested structure is about 96% in output power of 150W. The measured efficiency for the proposed topology is almost 95.5% at full load operation (input source is 20V and produced power is 170W). According to Fig. 13, it is clear that tolerance at the measured power level is not high in the presented converter. When the output power changes between 150W and 250W, the efficiency tolerance is about 1.4%. By increasing the diode-capacitor unit, the produced voltage and current levels are increased,



(a) (b)

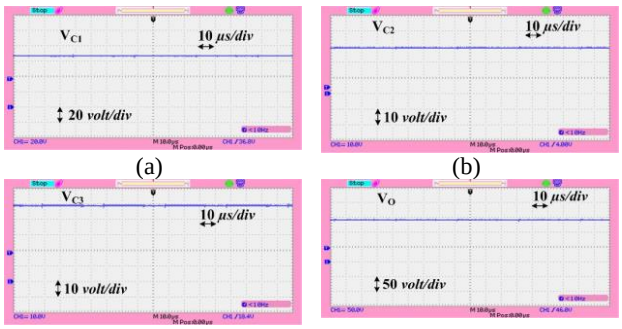
Fig. 10 Experimental measurement result of a) V_{Gate}, and b) V_{DS}.



(a) (b)

(c) (d)

Fig. 11 Experimental measurement result of input current and voltage of diodes: a) i_{in}, b) V_{D1}, c) V_{D2}, and d) V_{Do}.



(a) (b)

(c) (d)

Fig. 12 Experimental measurement results of capacitors voltage: a)V_{C1}, b) V_{C2}, c) V_{C3}, and d) V_{Co}=V_o.

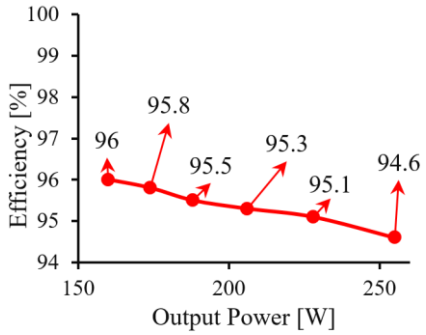


Fig. 13 Measured efficiency based on output powers.

therefore, the produced power level will be increased. It leads to improve the efficiency of the suggested converter for a similar power range.

7 Conclusion

In this study, a novel non-isolated high step-up boost DC-DC converter using a coupled inductor was proposed. The voltage conversion ratio of the presented converter is increased by adjusting the turn ratio of the coupled inductor. The main merits of the suggested converter consist of decreasing the number of cores (with integrated coupled inductor), achieve to high voltage gain with lower turn ratio, decreasing the peak voltage through the power switch by adjusting the turn ratio, and get a high efficiency (about 95.5% at 170W). The mathematical and experimental results verify each other and also, indicate that the proposed structure is a suitable as an interface converter for renewable applications like PV panels.

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