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Research Paper

A Minimal-Cost Inherent-Feedback Approach for Low-Power MRF-Based Logic Gates

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Abstract: The Markov random field (MRF) theory has been accepted as a highly effective framework for designing noise-tolerant nanometer digital VLSI circuits. In MRF-based design, proper feedback lines are used to control noise and keep the circuits in their valid states. However, this methodology has encountered two major problems that have limited the application of highly noise immune MRF-based circuits. First, excessive hardware overhead that imposes a great cost, power consumption and propagation delay on the circuits and second, separate implementation of feedback lines that adds further delay to the circuits. In this paper, we propose a novel approach for minimal-cost inherent-feedback implementation of low-power MRF-based logic gates. The simulation results, which are based on 32nm BSIM4 models, demonstrate that besides excellent noise immunity of the proposed method, it has the least propagation delay in comparison with all of the previously reported MRF-based gates due to its inherent feedbacks. In addition, the proposed method outperforms competing ones, which have comparable noise immunity, in other circuit metrics like cost and power consumption. Specifically, the proposed method achieves at least 18%, 29%, and 39% reductions in cost, delay and power consumption with considerable noise immunity improvement compared with competing methods.

Keywords: Noise Tolerance, Markov Random Field (MRF), Noise Immunity, Reliability.

1 Introduction

ONE of the major attributes of nanometer VLSI circuits is their low power consumption. The main factor that leads to this important attribute is the decrease in supply voltage since power consumption is proportional to the square of the supply voltage. This decrease makes the energy of intrinsic noise comparable to the energy difference between logic states in nanometer circuits and leads to interference of noise with desirable signals. The interference can be very serious when the circuits work in the subthreshold region. Noise fluctuation is and will be one of the most important concerns in VLSI circuits [1].

As the overall intrinsic noise is random, dynamic in nature and can occur anywhere in the circuits, the methods which deal with special types of noise such as crosstalk noise [2-4], power supply noise [5, 6], substrate noise [7, 8], ground bounce noise [9, 10] and IR drops [11, 12] cannot solve random noise interferences which are intrinsic to the circuits. Maintaining adequate noise margin and/or designing noise-tolerant circuits are the only ways to deal with intrinsic noise. As maintaining adequate noise margin is not usually possible in modern nanometer circuits, especially when they are in the subthreshold region, designing noise-tolerant circuits remains as the main or complementary solution to have noise immune circuits.

Due to stochastic behavior and inherency of noise in the whole circuit, probabilistic approaches provide a better platform for designing noise-tolerant circuits [13-16]. Probabilistic approaches can be applied to different levels of abstraction, however, circuit-level ones are more effective and easier to implement [16]. Among various probabilistic frameworks like Markov random field, Bayesian network (BN), probabilistic transfer matrices (PTM) and probabilistic decision diagrams (PDD), Markov random field has received

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great attention for designing noise-tolerant VLSI circuits [13-25]. In MRF-based circuits, noise energy is shared among the whole system and noise signal level is reduced noticeably. Therefore, noise tolerance is achieved.

Several MRF-based methods have been used for designing noise-tolerant circuits [13-25]. A straightforward method for mapping MRF design principles to VLSI circuits was proposed in [17, 18] for the first time. Because of the hardware complexity of the initial MRF-based design, most of the methods which have been proposed focused on techniques for reducing hardware overhead. Area efficient design [19], master-slave design [20], general cost-effective design for logic functions [21], area-sharing feedback NAND path [22], global mapping approach [23] and coding-based partial MRF [16] are the methods proposed to reduce the complexity of MRF-based designs. Although cost-effective methods have the advantage of lower hardware overhead, they usually sacrifice noise tolerance performance for hardware simplicity. Some methods used special techniques together with hardware simplification to compensate for the degradation of noise tolerance. A noise-tolerant logic design based on MRF theory and differential cascade voltage switch (DCVS) was proposed in [24]. I-Chyn Wey *et al*. used the Schmitt trigger circuit to improve the noise tolerance of their cost-effective MRF-based design in [25].

Although some efforts have been made in the previous works to simplify the hardware complexity of MRF-based circuits, the complexity is still the most important concern about these circuits. Unnecessary hardware overhead imposes an extra cost, delay, and power consumption together with reliability issues on the circuits that limit the application of noise immune MRF-based circuits. In addition, most of the reported works implemented feedback lines in a separate stage which in turn adds extra propagation delay to the circuits. Besides mentioned points, some of the reported methods sacrifice noise tolerance to achieve hardware efficient MRF-based circuits, which is unacceptable as the main advantage of these circuits is their great noise tolerance.

In this paper, we propose a Minimal-Cost Inherent-Feedback approach for designing low-power MRF-based noise-tolerant logic gates and name it MCIF-MRF. The circuit-level noise-tolerant design usually converges into the design of noise-tolerant logic gates as they are the basic components of VLSI circuits. Therefore, the proposed method is focused on designing noise-tolerant gates. The main contribution of this work is the notion of feedback inherency in state-generation and mutual participation of valid states in the construction of each other which leads to low cost, power-efficient and high-speed noise immune MRF-based circuits. The proposed method outperforms competing approaches in the aspects of circuit design including power, delay and cost and at the same time preserves superior noise tolerance.

The rest of this paper is organized as follows. Section 2 reviews MRF-based circuit designs. In Section 3, we explain the proposed minimal-cost inherent-feedback approach (MCIF-MRF) in detail. Section 4 presents various simulations and discussions to verify the design. This paper is concluded in Section 5.

2 Review of MRF-Based Circuit Designs

As mentioned before, the appropriate approach for dealing with intrinsic noise is the MRF-based design. In an MRF network, each signal can be considered as a node. The state of a node defines jointly by its neighborhood nodes. Through joint estimation, noise energy is shared between neighbor nodes and declined noticeably. Fig. 1 shows a typical circuit (full adder) and its corresponding MRF network.

In mapping a circuit onto an MRF network, nodes that have a logical relationship are fully connected together and form a clique. In this example, nodes A, B, and I1 form a clique and there are five cliques. To ensure the correct operation of a circuit, its joint probability should remain maximum for all times. According to the Hammersley-Clifford theorem, the joint probability is obtained from this equation [26]:

$$P(X) = \left(\frac{1}{Z}\right)\prod_{c\in C}\exp\left(\frac{-U_c}{kT}\right) \tag{1}$$

In this equation, C is the set of cliques, U_c is the clique energy function, and Z and kT are constants. To keep the joint probability maximum, the clique energy function should remain a minimum for each clique. This is a minimum for valid states of the corresponding clique. In logic circuits, cliques are related to logic gates. Therefore, to ensure maximum joint probability we should enforce the gates to be in their valid states. A common approach is to generate valid states and

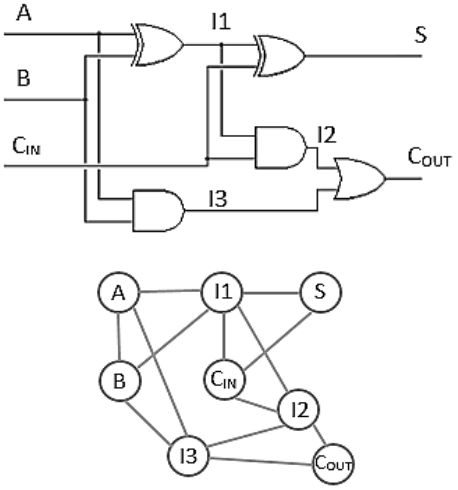


Fig. 1 A full adder circuit and its corresponding MRF network.

reinforce them with proper feedback lines.

The early work that used the MRF theory for designing noise-tolerant logic gates was proposed by Kundan Nepal *et al*. in [17]. In this work, which is known as direct mapping, all of the valid states were generated directly and reinforced by feedback lines. A similar design was used to implement an 8-bit carry-lookahead adder as the first MRF-based chip in [18]. The two-input NAND gate version of these designs are depicted in Fig. 2. For a two-input NAND gate, the valid state function (the summation of valid states) is $F=\overline{X0}X1X2+X0\overline{X1}X2+\overline{X0}\,\overline{X1}X2+X0X1\overline{X2}$, which X0 and X1 are inputs and X2 is output. As shown in Fig. 2, all of these valid states are generated and connected to appropriate nodes by feedback lines.

According to Fig. 2, the hardware complexity of these designs is very high so that they need 60 transistors for a two-input NAND gate. Therefore, although they have good noise immunity, their hardware overhead is unacceptable. To reduce the hardware complexity of the direct mapping approach, various methods have been proposed in recent years. Fig. 3 shows the two-input NAND gate version of the hardware efficient designs proposed recently. Fig. 3(a) shows the area efficient method which was proposed in [19]. In [20], I-Chyn Wey *et al*. pursued a different approach by separating state generation and feedback parts and named their work master-slave design which is shown in Fig. 3(b). This kind of approach continued in other works. In [25], the authors added the Schmitt trigger circuit to the master-slave design to benefit from Schmitt trigger noise reduction characteristics and enhance the noise immunity of the master-slave design as shown in Fig. 3(c). Kaikai Liu *et al*. proposed a design named CENT-MRF to reduce the hardware overhead of the master-slave design [21]. However, they completely removed one of the valid states that can degrade the noise tolerance performance of the circuit considerably. This design is shown in Fig. 3(d). To compensate for the noise tolerance degradation of the mentioned work, another design was proposed in [24]. In this design, a DCVS block was inserted in the middle of the CENT-MRF design as depicted in Fig. 3(d). Although adding such a block can improve noise tolerance, it imposes extra propagation delay on the circuit. Indeed, serial implementations like the DCVS-MRF design lengthen the critical path and lead to slower circuits.

All of the previously reported cost-effective approaches have the advantage of lower cost in comparison with the direct mapping approach. The state simplification in all of these methods is based on Boolean simplification, however, the type of state generation and reinforcement is different as shown in Fig. 3. The main drawback of the previous works is their non-comprehensive point of view in state-generation and reinforcement which deteriorates noise

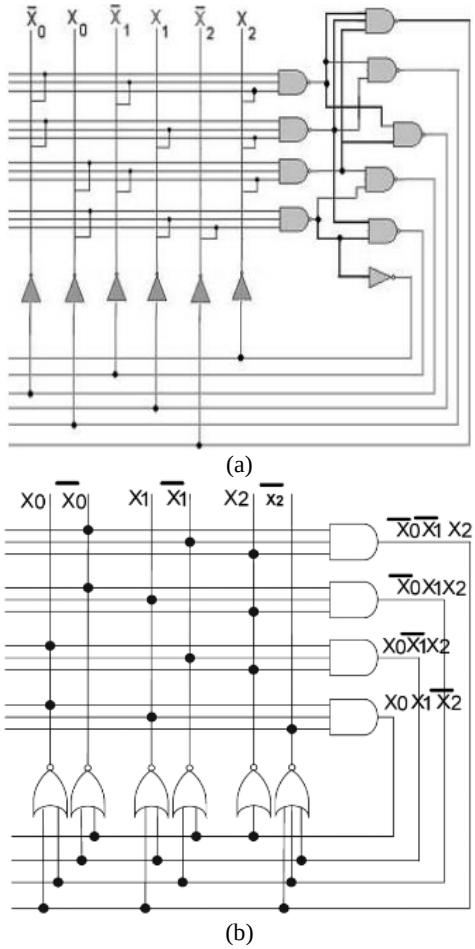


Fig. 2 Direct mapping MRF-based NAND gates; a) The first proposed design [17] and b) A similar design used to implement an MRF-based chip [18].

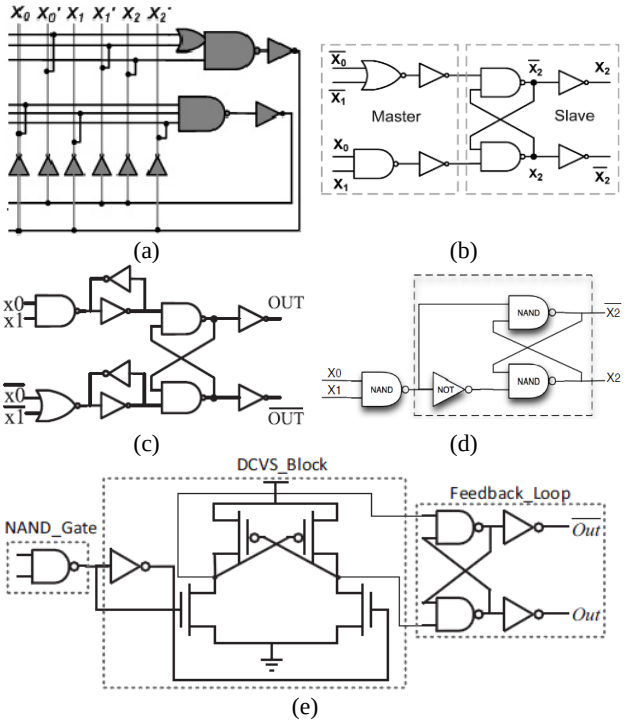


Fig. 3 Hardware efficient MRF-based NAND gates; a) Area efficient MRF [19], b) MS-MRF [20], c) Schmitt-MRF [25], d) CENT-MRF [21], and e) DCVS-MRF [24].

tolerance or important circuit metrics like cost, delay, and power. Therefore, an approach is required for modern low-power VLSI circuits to provide high levels of noise immunity with considerably low cost, delay, and power.

3 Minimal-Cost Inherent-Feedback Approach

The difference between MRF-based methods mainly relates to the mechanism of generating and reinforcing valid states that can directly affect the overall functionality and cost of the methods. In this paper, we propose a novel approach for generating and reinforcing valid states. This approach can be applied to all of the basic gates with no limitation on their inputs and leads to a minimal cost implementation that not only shows better noise tolerance but also is superior in other circuit metrics like power consumption and delay. In our approach, the simplified form of a valid state function is divided into two main valid states. These main valid states are implemented directly by using compound logic and they reinforce each other by participating in the construction of each other. Mutual participation of valid states in their construction and reinforcement is one of the main novelties of this work. Simplifying a valid state function and separating it into two main terms can be done for all of the basic gates with an arbitrary number of inputs as shown in Table 1.

Table 1 simply lists valid state functions and their two-part simplified forms for the basic gates. We will explain the mechanism of generating and reinforcing the main valid states of a two-input NAND gate. A similar method can be used for other basic gates with arbitrary inputs. The two main valid states can be implemented in their non-complement or complement forms. In the former, the first valid state generates output (y) and the second one generates output's complement ($\bar{y}$), and in the latter vice versa. We choose the second method and implement the complements of the two main valid states. For a two-input NAND gate, the complements of the valid states are $\overline{(\bar{x}1+\bar{x}2)}y$ and $\overline{x1x2\bar{y}}$ in order. We name these terms F1 and F2. These terms are implemented directly and participate in the construction of each other. Fig. 4 shows the implementation of a two-input NAND gate based on our proposed methodology. Fig. 4(a) is the transistor level representation and Fig. 4(b) is the block diagram of the design that can be generalized to all types of basic gates with an arbitrary number of inputs.

Table 1 Valid state functions and their simplified forms for various basic gates.

Basic gates	Valid state functions (x is input and y is output)	The simplified form of the valid state functions in an arranged two-part form
NOT	$F=\bar{x}y+x\bar{y}$	$F=\bar{x}y+x\bar{y}$
NAND2	$F=\bar{x}1x2y+x1\bar{x}2y+\bar{x}1\bar{x}2y+x1x2\bar{y}$	$F=(\bar{x}1+\bar{x}2)y+x1x2\bar{y}$
NOR2	$F=\bar{x}1\bar{x}2y+\bar{x}1x2\bar{y}+x1\bar{x}2\bar{y}+x1x2\bar{y}$	$F=\bar{x}1\bar{x}2y+(x1+x2)\bar{y}$
NAND3	$F=\bar{x}1x2x3y+x1\bar{x}2x3y+x1x2\bar{x}3y+\bar{x}1\bar{x}2x3y+\bar{x}1x2\bar{x}3y+x1\bar{x}2\bar{x}3y+\bar{x}1\bar{x}2\bar{x}3y$ $+x1x2x3\bar{y}$	$F=(\bar{x}1+\bar{x}2+\bar{x}3)y+x1x2x3\bar{y}$
NOR3	$F=\bar{x}1x2x3\bar{y}+x1\bar{x}2x3\bar{y}+x1x2\bar{x}3\bar{y}+\bar{x}1\bar{x}2x3\bar{y}+\bar{x}1x2\bar{x}3\bar{y}+x1\bar{x}2\bar{x}3\bar{y}+\bar{x}1\bar{x}2\bar{x}3\bar{y}$ $+\bar{x}1\bar{x}2\bar{x}3y$	$F=\bar{x}1\bar{x}2\bar{x}3y+(x1+x2+x3)\bar{y}$
NANDn	$F=\bar{x}1x2\ldots xny+\ldots+\bar{x}1\bar{x}2\ldots xny+\ldots+\bar{x}1\bar{x}2\ldots\bar{x}ny+x1x2\ldots xn\bar{y}$	$F=(\bar{x}1+\bar{x}2+\ldots+\bar{x}n)y+x1x2\ldots xn\bar{y}$
NORn	$F=\bar{x}1x2\ldots xn\bar{y}+\ldots+\bar{x}1\bar{x}2\ldots xn\bar{y}+\ldots+x1x2\ldots xn\bar{y}+\bar{x}1\bar{x}2\ldots\bar{x}ny$	$F=\bar{x}1\bar{x}2\ldots\bar{x}ny+(x1+x2+\ldots xn)\bar{y}$

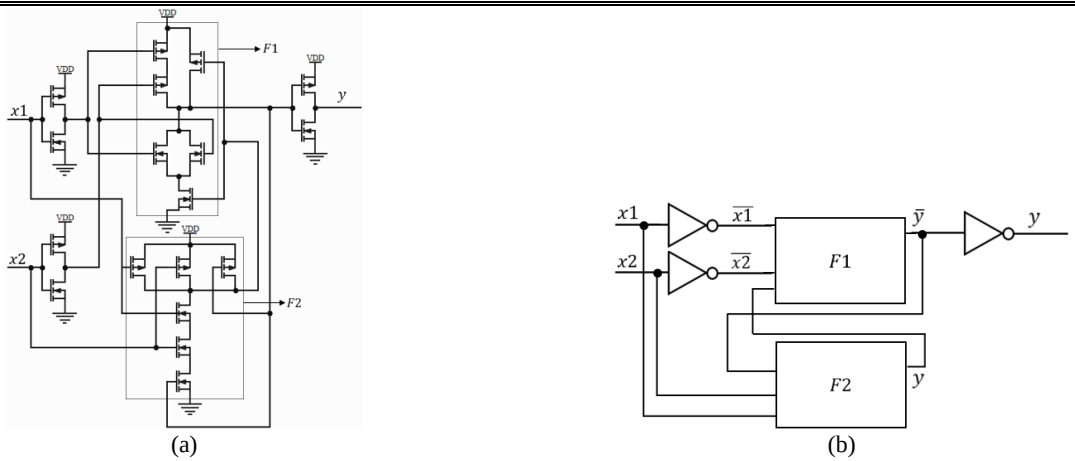


Fig. 4 The implementation of the proposed MRF-based design for a two-input NAND gate; a) Transistor level representation and b) Block diagram representation.

In general form, F1 and F2 are the complements of the first and second main valid states and can have a different number of inputs depending on the number of gate's inputs. The NOT gates on the left side of Fig. 4(b), are also proportional to the inputs and generate the complements of them. Therefore, each additional input adds only six transistors to the design (2 for a NOT gate, 2 for F1 and 2 for F2). This is a very important property of the proposed approach that the design has the same structure for all types of basic gates and can be extended to the gates with a higher number of inputs by adding a limited and constant number of transistors. There is a single NOT gate on the right side of the figure that restores y from $\overline{y}$ and does not depend on the gate's type and the number of inputs. Restoring output from its complement rather than using its computed value at the output of the F2 unit has a design reason. When inputs are noisy, the F1 unit can generate a more stable signal compared with the F2 unit because the inputs pass through two restoring logics (NOT gates and F1 unit) to reach F1 output but they only pass through one restoring logic (F2 unit) to reach F2 output. The restoring logic is a circuitry designed so that even with an imperfect input signal, a standard output occurs at the exit. Since the NOT gates, F1 unit, and F2 unit conform to the CMOS rules, they are considered fully restoring logics. Therefore, the signal $\overline{y}$ is a stronger signal and through passing the final NOT gate forms the output signal. In the proposed structure, the whole circuit requires only 18 transistors for a two-input NAND gate and has the least hardware overhead in comparison to previously reported MRF-based circuits that have comparable noise immunity. Contrary to the previous methods, in our proposed method the mechanism of controlling noise is inherent in the design. It means that the feedback lines which control the energy of the circuit are integrated into the state generation to form a united structure. The minimal-cost and inherent-feedback properties of the proposed method lead to various design merits that will be investigated in the next section.

The methodology, which was explained for a two-input NAND gate in detail, can be generalized simply to any type of logic gates with arbitrary inputs. First, the valid state function is defined and simplified in a two-part form (like Table 1). Second, similar to the mentioned procedure, the simplified terms are implemented directly using compound logic in a way that each one contributes to the implementation of the other.

The next section presents various simulation results and discussions that prove high noise tolerance and superior performance of the proposed method in terms of main circuit metrics like cost, power consumption, and delay.

4 Simulation Results and Design Verification

All of the simulations in this section were performed in the Hspice platform with a 32nm library based on the BSIM4 models [27]. Since the main concern about noise interference is for low-power subthreshold circuits, all of the circuits were biased in their subthreshold region to demonstrate the noise immunity of the circuits effectively. The threshold voltage is 0.5V and we chose 0.2V for the supply voltages of the circuits. To ensure the presence of thermal noise, the temperature was set to 50°C. As the best model for intrinsic noise is additive white Gaussian noise, we used this model with uniform distribution and various signal to noise ratios (SNRs) to generate noisy signals.

Design verification is presented in three phases. First, we monitor the output of various MRF-based two-input NAND gates with noisy inputs to evaluate their noise tolerance. Then, bit error rate (BER) values for all of the gates in a wide range of SNR and the important circuit metrics of the gates are presented. Second, noise tolerance evaluation, bit error rate computation and circuit metrics simulations are provided for a 4-bit ripple carry adder (RCA) to demonstrate the performance of the MRF-based gates in a bigger and operational module. Third, the effects of process variations on the proposed gate are investigated by the Monte Carlo simulation results to evaluate the robustness and performance of the gate on account of variations.

We exclude the direct mapping and area-efficient (Fig. 3(a)) approaches from our discussions. These methods require an excessive number of transistors (60 and 36 respectively) for their implementations and consequently consume considerable power. In addition, the design in Fig. 3(a) has an asymmetric structure in state generation which can lead to timing violations. Therefore, they are not appropriate for modern low-power circuits and are kept out of comparison.

Fig. 5 shows the outputs of various MRF-based two-input NAND gates together with the traditional CMOS gate in the presence of noisy inputs with 6dB SNR. As shown in this figure, the traditional CMOS gate loses its correct functionality and its output toggles between logic levels. On the contrary, the MRF-based gates show considerable noise tolerance, especially DCVS-MRF, Schmitt-MRF and our proposed gate (MCIF-MRF) which have superior noise tolerance among others. This figure can clarify that when the circuits are in their subthreshold region and are exposed to noise, an MRF-based design can be a highly effective solution for the circuits' correct operation.

The precise ability of various MRF-based gates in terms of noise tolerance is depicted in Fig. 6. In this figure, bit error rate (BER) results for various designs in a wide range of SNR are shown. In Fig. 6(a), the input SNR range covers 2dB to 7dB signal to noise ratios with 0.5 dB steps. For clear observation of noise tolerance performance in higher SNRs, Fig. 6(b) is depicted as a close view of Fig. 6(a) in 5dB to 7dB range. If we put aside CMOS (non-MRF) and CENT-MRF methods,

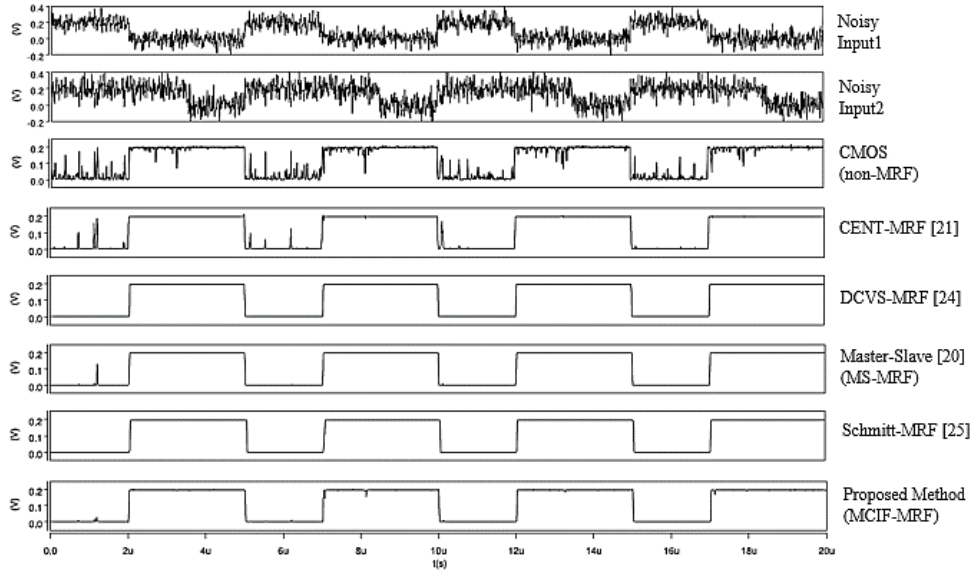
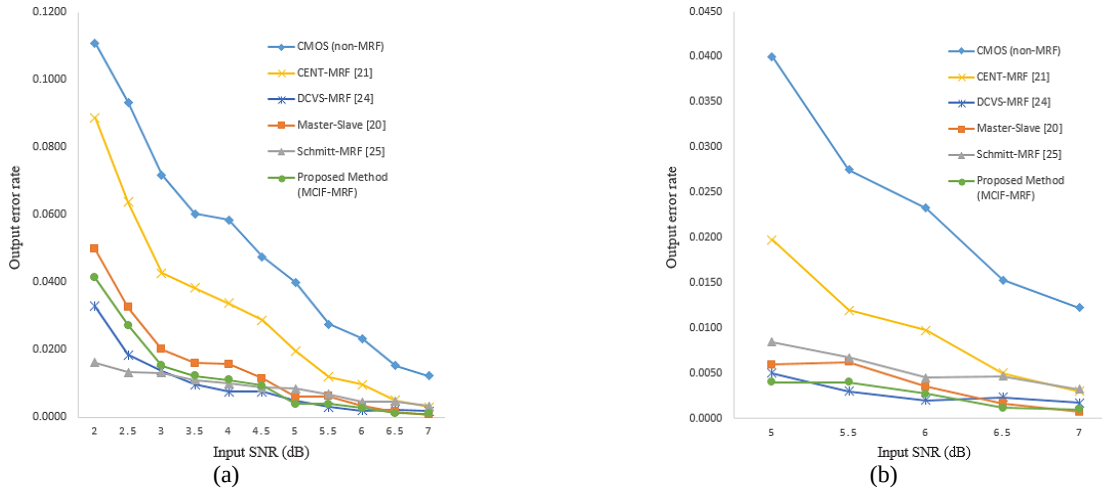


Fig. 5 The inputs and outputs of various MRF-based two-input NAND gates and the traditional CMOS gate.



(a) (b)

Fig. 6 Output error rates in the presence of noisy inputs with different SNRs for various designs; a) Input SNR ranges from 2dB to 7dB and b) Input SNR ranges from 5dB to 7dB.

other ones show comparable noise immunity. The weak performance of the CENT-MRF method (especially in lower SNRs) is due to the omission of one valid state and the lack of a compensation mechanism.

In Table 2, the cost in terms of transistor count (TC), propagation delay, power consumption, average bit error rate and the average percentage of noise immunity improvement versus CMOS in different SNR ranges are provided. As shown in the table, the proposed MCIF-MRF method has the least propagation delay among all of the previously reported MRF-based methods. This valuable achievement is due to the innovative notion of inherent feedbacks which prevents an extra stage for feedback lines and results in a high-speed circuit. The proposed method not only is superior in speed but also outperforms competing methods that have comparable noise tolerance (shown in the bolded rectangle) in cost and power consumption. Moreover, in higher SNRs, it has the best performance in noise tolerance and demonstrates more than 9 times (912%) noise immunity improvement versus CMOS method.

The proposed method shows at least 18%, 29%, and 39% reductions in cost, delay, and power consumption respectively in comparison with competing methods. We achieved these major reductions without any valid state omission and at the same time obtained superior noise tolerance, especially in higher SNRs.

To evaluate the circuit metrics and noise tolerance performance of various methods in a bigger and operational unit, a 4-bit ripple carry adder (RCA) was used. Fig. 6 shows the noise tolerance performance of various MRF-based and CMOS 4-bit ripple carry adders in the presence of noisy inputs with a 5dB signal to noise ratio. The input carry of the first stage and data lines are noisy and the output carry of the fourth stage is monitored as the circuit output. The electrical path between the first input carry and the last output carry is the critical path of an RCA and is affected by all of the

Table 2 Circuit metrics for various two-input NAND gate designs.

Design	Cost (TC)	Delay [ns]	Power [pw]	Average BER (2-7)	Average BER (5-7)	The average percentage of noise immunity improvement versus CMOS* (2-7)	The average percentage of noise immunity improvement versus CMOS (5-7)
CMOS (non-MRF)	4	8.96	86.01	0.0510	0.0237	-	-
CENT-MRF [21]	14	31.21	321.44	0.0314	0.0099	162%	239%
DCVS-MRF [24]	22	37.81	657.26	0.0095	0.0028	537%	846%
MS-MRF [20]	28	37.80	826.89	0.0149	0.0036	342%	658%
Schmitt-MRF [25]	32	70.61	1129.80	**0.0091**	0.0055	**560%**	431%
MCIF-MRF (Proposed method)	**18**	**26.86**	**402.75**	0.0118	**0.0026**	432%	**912%**

* (average BER of CMOS/average BER of corresponding design)×100

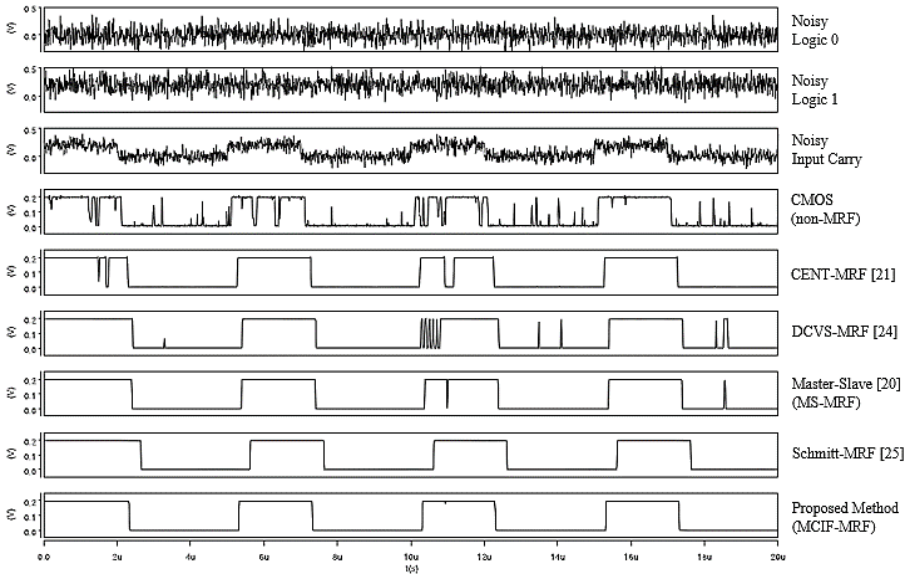


Fig. 7 The inputs and outputs of various 4-bit RCAs.

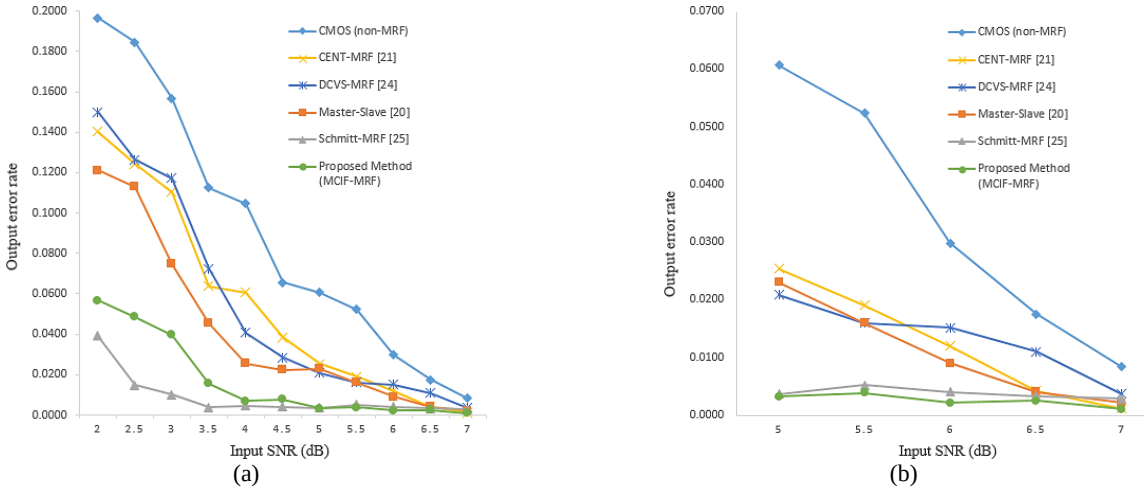


Fig. 8 Output error rates of different 4-bit RCAs in the presence of noisy inputs with different SNRs; a) Input SNR ranges from 2dB to 7dB and b) Input SNR ranges from 5dB to 7dB.

inputs. Therefore, it is used for a better demonstration of noise tolerance. Because of several noisy inputs in a bigger and operational module like 4-bit RCA (9 noisy inputs: 8 data lines and input carry), it can show the noise tolerance capability of methods more effectively.

As shown in Fig. 7 the traditional CMOS method is completely out of work and the MRF-based methods demonstrate superior noise immunity. However, the proposed method and Schmitt-MRF method show great operation. The propagation delay difference of various adders can be observed in this figure. A detailed analysis of various adders' performance is presented in this section. Fig. 8(a) depicts the output error rate of various methods in the presence of noisy inputs in a

wide range of SNRs. The figure clearly displays the noise tolerance capability of the proposed method and the Schmitt-MRF method. Fig. 8(b) is a close view of Fig. 8(a) in higher SNRs. It clarifies that the best operation in noise tolerance when the noisy inputs have higher SNRs belongs to the proposed method. In addition to the noise tolerance merits of the proposed method, its low power consumption, minimal cost structure and high-speed characteristic due to inherent feedbacks, highlight it among competing methods.

Table 3 provides circuit metrics and bit error rate results in different SNR ranges for various 4-bit ripple carry adders. In this case, the competing methods in noise tolerance ability are the proposed method and Schmitt-MRF method which are in the bolded rectangle. The former is superior in higher SNRs and the latter performs better in lower ones. However, the proposed method completely outperforms the competing one in cost, delay, and power which are very important circuit metrics. Specifically, the proposed method is highly power efficient and consumes 64% less power. In addition, there are 44% and 48% reductions in cost and delay respectively. If we compare our method with master-slave MRF which is another well-known method in the literature, it shows 36%, 18%, and 51% reductions in cost, delay, and power consumption in order. At the same time, it achieves 243% and 432% noise immunity improvements versus the master-slave method in different SNR ranges.

The effects of process variations on the proposed gate were investigated by a Monte Carlo simulation with Gaussian distribution, 10% relative variation and 3 sigmas (3σ) that is common in the literature [28]. The channel length and width of the transistors were selected as the parameters of the Monte Carlo simulation. Accordingly, the effective length and width (L_{eff}, W_{eff}) of the transistors were used in the simulations rather than their nominal ones. The Monte Carlo simulation was repeated 30 iterations and the proposed gate simulated for each iteration with random values of L_{eff} and W_{eff}. Fig. 9(a) shows the gate's output in the presence of noisy inputs with 6dB SNR. The nominal signal shows the output when the transistors have their nominal values for L and W and the Monte Carlo one demonstrates the outputs produced by the Monte Carlo simulation for all of the iterations.

Table 3 Circuit metrics for various 4-bit ripple carry adder designs

Design	Cost (TC)	Delay [ns]	Power [nw]	Average BER (2-7)	Average BER (5-7)	The average percentage of noise immunity improvement versus CMOS (2-7)	The average percentage of noise immunity improvement versus CMOS (5-7)
CMOS (non-MRF)	144	99.13	3.52	0.0899	0.0337	-	-
CENT-MRF	504	275.95	11.68	0.0545	0.0123	165%	274%
DCVS-MRF	792	403.54	23.47	0.0547	0.0133	164%	253%
MS-MRF	1008	387.34	29.53	0.0415	0.0108	217%	312%
Schmitt-MRF	1152	610.84	40.05	**0.0087**	0.0038	**1033%**	887%
MCIF-MRF (Proposed method)	**648**	**316.50**	**14.54**	0.0171	**0.0025**	520%	**1348%**

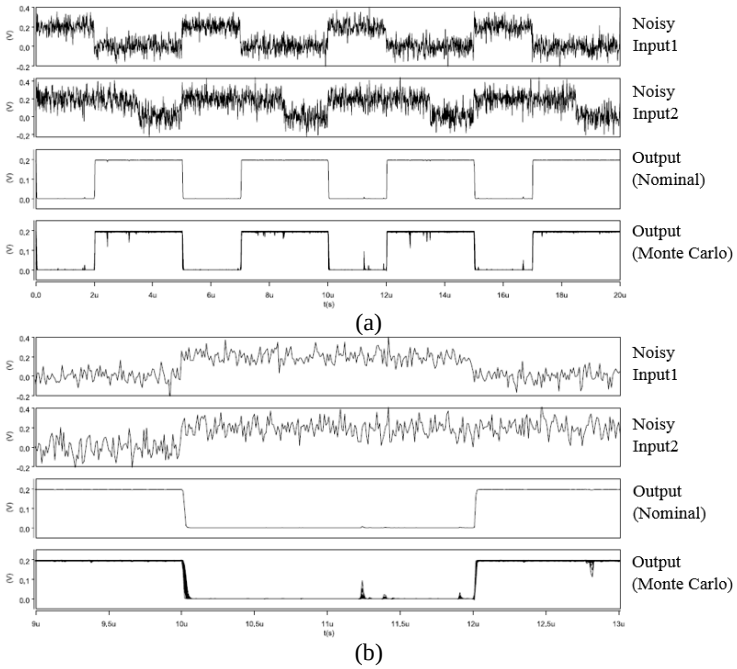


Fig. 9 The inputs and output of the proposed NAND gate in the nominal and Monte Carlo states; a) The interval between 0 and 20 microseconds and b) A closer view between 9 and 13.

Table 4 Circuit statistics for the proposed gate in the Monte Carlo simulation.

Statistics	Propagation Delay	Power Consumption
Mean	28.2857E-9	444.7433E-12
Variance	4.6297E-18	2.1770E-21
Standard deviation (sigma)	2.1517E-9	46.6589E-12

As shown in Fig. 9(a), the proposed gate can successfully tolerate the process-induced variations on the length and width of the transistors. In a very limited number of iterations, the output deviates from its ideal value that can be seen more clearly in Fig. 9(b). This figure shows the outputs from 9 to 13 microseconds. The effects of process variation on the gate's circuit metrics are presented in Table 4.

In Table 4, the important statistics for the propagation delay and power consumption are provided. The slight variance values show that most of the delay and power values are very close to the mean. It means that the process variations have a limited impact on the metrics of the proposed MRF-based gates.

By considering the mentioned discussions, it can be concluded that the proposed method paves the way for low cost, power-efficient and high-speed noise immune MRF-based circuits which are necessary for reliable circuit design. To the best of our knowledge, this work is the first hardware efficient approach that provides high levels of noise immunity with considerably low cost, delay, and power.

5 Conclusion

In this paper, we proposed the MCIF-MRF method for designing efficient noise-tolerant circuits. The proposed method is low-power, cost-effective, high speed and more reliable in comparison with competing methods and provides a practical tradeoff between noise immunity and circuit metrics. According to the noise susceptibility of modern VLSI circuits, using noise-tolerant circuits will be inevitable especially in critical applications and the proposed method can be a worthy successor for existing MRF-based methods.

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