IUST
Iran University of Science and Technology

Iranian Journal of Electrical and Electronic Engineering

Journal Homepage: ijeee.iust.ac.ir

Research Paper

A Buck-Boost Converter; Design, Analysis and Implementation Suggested for Renewable Energy Systems

H. Shayeghi*(C.A.), S. Pourjafar*, and F. Sedaghati*

Abstract: This work introduces a new non-isolated buck-boost DC-DC converter. Interleaved configuration of the suggested structure increases the voltage conversion ratio. The voltage rate of the suggested converter can be stepped-up and stepped down for lower values of duty-cycle, which causes to decrease in the conduction losses of the system. The voltage conversion ratio of the recommended structure is provided with low maximum voltage throughout the semiconductor elements. Additionally, utilizing only one power switch facilitates converter control. Using a single power MOSFET with small conducting resistance, $R_{DS\text{-}ON}$, increases the overall efficiency of the recommended topology. To verify the performance of the presented converter, technical description, mathematical survey, and comparison investigation with similar structures are provided in the literature. Finally, a laboratory scheme with a 100W load power rate at 50 kHz switching frequency is carried out to demonstrate the effectiveness of the proposed converter.

Keywords: Buck-Boost Converter, Low Peak Voltage, High Efficiency, Single Switch.

1 Introduction

1.1 Background

IN recent years, the lack of fossil fuels and environmental issues have received the main consideration in order to access green energy and usage of renewable power resources like photovoltaic (PV) generation, fuel cell, and wind power [1-3]. In most systems for instant battery charging and discharging, power factor correction, fuel cell voltage adjustment, DC bus voltage regulation in wind turbines with synchronous generator, uninterruptible power supplies (UPS) voltage regulation, a DC-DC converter is required to provide a regulated output voltage from an unadjusted voltage resource [4, 5]. Since all semiconductors are powered by DC sources, these converters are found in almost all of today's electronic devices. When the adjusted voltage is within the rate of the unchanged source voltage, a buck-boost structure is needed [6]. The buck-boost converter is a type of switching converter that incorporates the buck and boost circuit principles into a single circuit that provides a regulated output voltage from a DC voltage [7-9]. There are various power supplies, such as batteries, which their output voltage depends on the power supply, and in this case, the circuit is needed to reduce the source voltage if its voltage is high and increase the source voltage if its voltage is poor as mentioned in [10, 11].

1.2 Literature Review

Buck-boost converters with only one switch for instant conventional buck-boost, Flyback, SEPIC and CUK have high peak voltage throughout the semiconductors and low efficiency [12, 13]. The mentioned converter in [12] has a single switch that leads to making the simple control unit. Also, the produced load voltage of this converter is higher than the conventional boost, buck-boost, CUK, and SEPIC converter. However, the main drawbacks related to this converter are high input current ripple and high losses because of using a large number of semiconductor elements with hard switching condition. The converter in [13] integrated buck-boost converter for achieving a

Iranian Journal of Electrical and Electronic Engineering, 2021.
Paper first received 22 April 2020, revised 10 June 2020, and accepted 17 June 2020.
* The authors are with the Energy Management Research Centre, University of Mohaghegh Ardabili, Ardabil, Iran.
E-mails: hshayeghi@gmail.com, saeedpourjfar22@gmail.com, and farzad.sedaghati@uma.ac.ir.
Corresponding Author: H. Shayeghi.
https://doi.org/10.22068/IJEEE.17.2.1862

high voltage conversion ratio. This structure can increase the output voltage rate in four steps. However, in this converter, the power losses are very high due to using magnetic components with high leakage inductance. Also, the dynamic behavior of this converter is complex because of using magnetic coupling. A high gain buck-boost converter with high voltage gain and low voltage stress is introduced in [14]. Although the maximum voltage throughout the semiconductors of this structure is low, the efficiency is low and the cost of the converter is high because of using a large number of passive and active components. Besides, it is difficult to model the average model of the mentioned converter for controlling the converter. In [15, 16] the buck-boost converters with interleaved configuration are presented. The voltage rate of the mentioned topology is high. The converter [16] can be controlled without using an auxiliary circuit in other word tits control systems is simple. But it has high ripple content through the semiconductors. In addition, the peak voltage through the switch of converters [15, 16] is high. In [17] a new control of interleaved buck-boost converter in electric vehicle battery application has been described. Although this control method can smooth the current peak of the battery, the control unit is complex and the cost is very high. A bidirectional buck-boost converter with soft switching capability has been mentioned in [18]. The proposed converter can transfer energy from source to load and also from load to source. Although the presented converter has a high voltage conversion ratio, the control strategy because of using coupled inductor and four active switches. Besides, it has a large number of components that lead to decreasing efficiency and the system cost will be high. The non-inverting buck-boost structure has been mentioned in [19] which has been recommended for fuel cell systems. The main features of the converter are as 1) the common ground problem is solved, 2) low number of components are utilized and 3) the output rippled content is decreased because of using interleaved technique. However, the efficiency of the suggested topology is low, the voltage stress of the switch is high and also the control of the mentioned converter is difficult because of using three switches. The mentioned converter in [20] is a quadratic buck-boost converter with low ripple content through output current. Although such structures are capable of working in high voltage applications because of using quadratic voltage gain, their control systems are complicated and the system cost is high. The converters in [21-23] are single switch buck-boost converter that they have more advantages such as better efficiency, simple structure with simple control and higher power density. However, the fundamental issue related to these topologies is the high peak voltage of switches and also, the input voltage variations cannot be made over a wide range. There is another buck-boost converter based on switching capacitor technique, which has been proposed in [24]. This buck-boost converter can get relevant voltage gain with low current ripple content which leads to decreasing the EMI noise. However, this converter is operating in hard switching condition that leads to increase the losses of the power converter and also it has large peek voltage throughout the switch.

1.3 Contribution

In order to overcome the related drawback of mentioned converters, the new structure of buck-boost converter should be defined with specification such as a high voltage conversion ratio in both step-up and step-down mode, lower peak voltage through the semiconductors and also soft-switching condition in order to be an appropriate candidate in low power renewable energy systems.

This paper suggests a new buck-boost converter with high voltage conversion ratio in both step-up and step-down modes. The main features of the recommended structure are indexed as follows:

- High voltage rate among the conventional buck-boost, SEPIC, and CUK converters;
- Lower peak voltage throughout the semiconductors;
- High efficiency because of the existence of a soft-switching condition;
- Simple control of the recommended structure because of using a single switch.

The voltage gain of the recommended structure is high. Moreover, in the suggested topology, the peak voltage through the is low and the overall efficiency is high. Additionally, there is only a single switch in the suggested converter, which facilitates the converter control design. The operation description of the suggested converter and its mathematical analysis are prepared in this study. Also, to prove the proficiency of the recommended topology, technical description and comparison survey with similar topologies are given in the literature. Conclusively, to demonstrate the features of the recommended topology, a laboratory scheme with a 100 W load power rate and 50 kHz operating frequency is fabricated.

2 Operation of the Suggested DC-DC Converter

The circuit scheme of the suggested converter is depicted in Fig. 1. The recommended converter includes a DC supply in the input side, a single active switch, three diodes, three inductors, and five capacitors. The combination of the inductors, capacitors, and diodes operates as a voltage multiplier unit, which increases the voltage conversion ratio and subsequently decreases the voltage stress of the semiconductors. To have a simple analysis of the presented converter, some presumptions are remarked in the following:

- The DC resource has constant value;
- The capacitors are considered to be large enough as the capacitors voltage ripple is low in the

switching period;

- Equivalent series resistance (ESR) of elements are ignored. So, they are considered ideal;
- The transient time interval is ignored.

Two operation modes are supposed for each period of switching (T_s). In the first operation time, the switch is in ON-state (dT_s) and in the second time interval, the main switch is going to OFF-state ((1-d)T_s).

2.1 Operation in Continuous Conduction Mode (CCM)

The main waveforms of the circuit operation in CCM are indicated in Fig. 2(a). As depicted in this figure, two states are remarked for the circuit operation, which are described in the following:

Mode 1: In this mode, the main switch is turned on by signaling the gate-source voltage. Diodes D_1, D_2, and D_o are blocked via voltages v_{c3}-v_{in}, v_{c2}+v_{c4}-v_{in}, v_{c1}-v_o-v_{in}, respectively. The inductors L_1, L_2, and L_3 start to be charged by transferring energy from input DC supply and capacitors C_1 and C_2. Therefore, the inductor current increases linearly, which is indicated in Fig. 2(a). The capacitors C_1 and C_2 are charged via currents I_{in}+i_{L1}-i_{c2} and I_{in}-i_{L1}-i_{c1}, respectively. The capacitors C_3, C_4, and C_o discharge in this time interval. The capacitor C_B is charged in this mode via input source and also transfer input energy to the inductor L_B and leads to charge it. The related equivalent prototype with this mode has been illustrated in Fig. 2(b). The following equations are given for this mode of operation:

$$v_{L1} = V_{in} \tag{1}$$
$$v_{L2} = V_{in} + V_{C3} - V_{C2} \tag{2}$$
$$v_{L3} = V_{in} + V_{C4} - V_{C1} \tag{3}$$
$$v_{LB} = V_{CB} - V_{C1} \tag{4}$$

Mode 2: In this mode, diodes start to conduct and the main switch is blocked. The inductors current is decreased linearly and it started to discharge. The capacitors C_3, C_4, and C_o are charged with transferring energy via inductors L_2, L_3, and current i_{Do}-I_o, respectively. Also, the capacitors C_1 and C_2 discharge in this time interval. In addition, the diode D_2 starts to conduct softly, which demonstrates the zero voltage switching (ZVS) condition of the recommended structure. The current direction of this mode is indicated in Fig. 2(c). In this operation time, the current stress throughout the diode D_o is suppressed by inductor L_B and decreases the conduction losses of diode D_o. The absorbed energy in capacitor C_B is transferred to the load and increases the voltage gain in boost mode. Due to this figure, the following equations are derived:

$$v_{L1} = -V_{C3} = V_o - V_{C1} = V_{C4} - V_{C2} \tag{5}$$
$$v_{L2} = -V_{C2} = V_{C3} - V_{C4} = V_{C2} - V_{C1} + V_o - V_{C3} \tag{6}$$
$$v_{L3} = V_{C4} - V_o = V_{C2} - V_{C3} = V_{C4} - V_{C3} - V_{C1} \tag{7}$$
$$v_{LB} = V_o + V_{C2} - V_{C4} - V_{C1} \tag{8}$$

By utilizing the volt-second balance principle for the inductors, the capacitor voltages are calculated as follows:

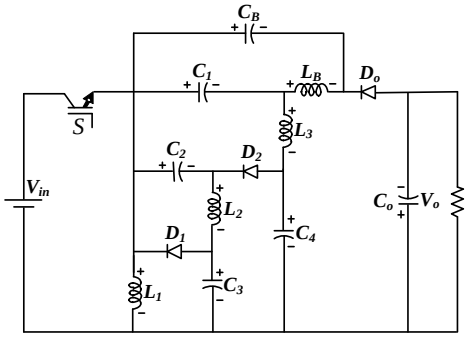


Fig. 1 The power circuit of the recommended structure.

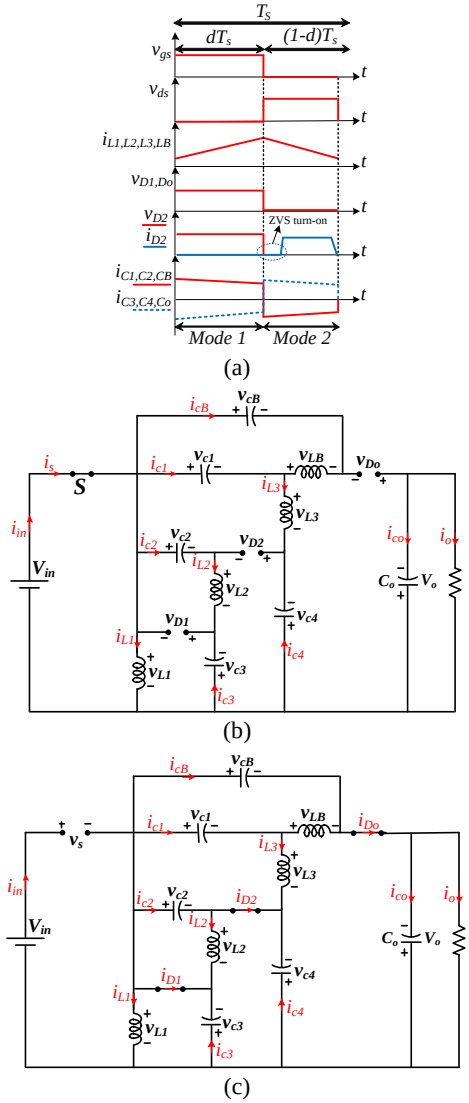


Fig. 2 The operation principle of the recommended structure; a) basic waveforms of the presented structure in CCM,

b) related circuit with mode 1, and c) related circuit with mode 2.

$$V_{C1}=V_{C4}=V_{CB}=\frac{2d}{1-d}V_{in} \tag{9}$$

$$V_{C2}=V_{C3}=\frac{d}{1-d}V_{in} \tag{10}$$

Also, the voltage gain in CCM (M_{CCM}) can be defined as follows:

$$M_{CCM}=\frac{V_o}{V_{in}}=\frac{I_{in}}{I_o}=\frac{3d}{1-d} \tag{11}$$

The suggested converter can be operated in both buck and boost states by expressing the duty cycle value for the voltage conversion ratio in CCM, as follows:

$$M=\begin{cases}\dfrac{3d}{1-d}\geq 1\rightarrow d\geq\dfrac{1}{4}\Rightarrow \text{Boost state}\\ \dfrac{3d}{1-d}\leq 1\rightarrow d\leq\dfrac{1}{4}\Rightarrow \text{Buck state}\end{cases} \tag{12}$$

The semiconductor elements are one of the major parts of the DC-DC converters. Typically, the semiconductor element, such as switch and diode is conducting and blocking in hard switching conditions. The hard switching condition has some drawbacks such as high switching losses, high peak voltage through the semiconductors, limitation on the operating frequency, and high electromagnetic interference (EMI). To overcome these problems, the soft-switching condition can be utilized in power converters. By using soft switching conditions such as ZVS and ZCS, the switching losses and EMI can be decreased intensity, and subsequently, the overall efficiency of the converters can be increased. In the suggested converter, a zero voltage switching in Off state is occurring for a diode. In this case, before the main diode started to change the situation from off-state to on-state, the diode started to conduct. With this feature, the switching losses and reverse recovery losses of diode D_2 be completely eliminated, and also the overall efficiency of the recommended converter can be increased.

2.2 Operation in Discontinuous Conduction Mode (DCM)

When the stored energy in the inductors is depleted completely and their currents reach zero, the converter will be operated in DCM. Thus, the DCM operation is defined for the proposed structure by considering three modes. The main waveforms of this mode are indicated in Fig. 3(a). As depicted in this figure, the first and the second switching state of DCM are similar to the CCM. However, in the third switching state, the switch and diodes are off and inductors current reach zero. The related equivalent prototype of the third mode has been demonstrated in Fig. 3(b). By using the volt-second balance law for the inductors, the capacitor voltage in DCM operation can be expressed as follows:

$$V_{C1}=V_{C4}=V_{CB}=\frac{dV_{in}+d'V_o}{d'} \tag{13}$$

$$V_{C2}=V_{C3}=\frac{d}{d'}V_{in} \tag{14}$$

So, the voltage conversion ratio in DCM (M_{DCM}) can be expressed as follows:

$$\frac{V_o}{V_{in}}=\frac{d}{d'} \tag{15}$$

$$d'=\frac{dV_{in}}{V_o} \tag{16}$$

According to the previous section, it is obvious that the average current of diodes is equal to the average current of the inductors that is equal to the output average current. Therefore, the following relations can be written:

$$I_{D1}+I_{D2}+I_{Do}=I_{L1}+I_{L2}+I_{L3}=3I_o \tag{17}$$

According to Figs. 3(a) and 2(b) and by considering that $I_o=V_o/R$, we have:

$$I_{D1}=I_{D2}=I_{Do}=\frac{V_o}{R} \tag{18}$$

$$3\frac{V_o}{R}=\frac{1}{2}d'I' \tag{19}$$

where I' is equal to the summation of the maximum current of all inductors and is defined as follows:

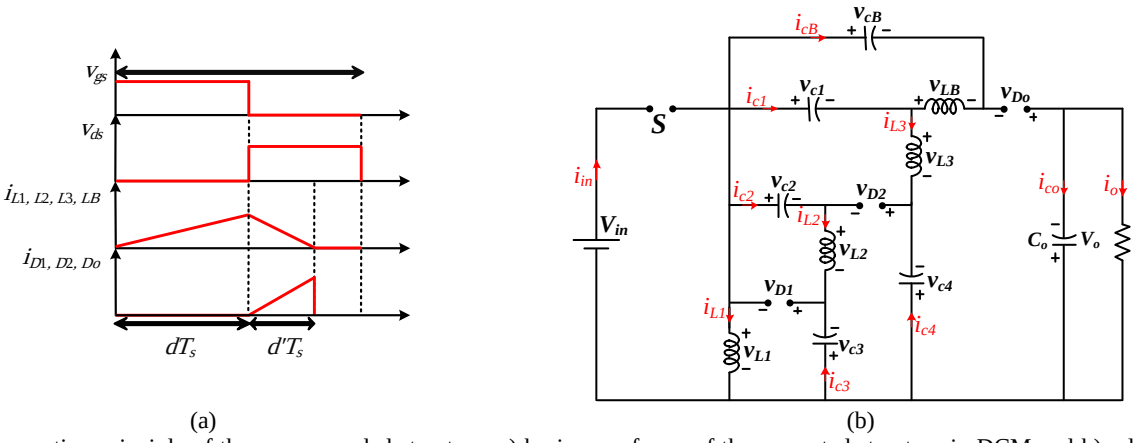
$$\begin{cases}I'=I_{L1}+I_{L2}+I_{L3}=\dfrac{V_{in}dT_S}{L_{tot}}\\ \dfrac{1}{L_{tot}}=\dfrac{1}{L_1}+\dfrac{1}{L_2}+\dfrac{1}{L_3}\end{cases} \tag{20}$$

By substituting (18) and (19) into (20), we have:

$$3\frac{V_o}{R}=\frac{1}{2}d'\left(\frac{V_{in}dT_S}{L_{tot}}\right) \tag{21}$$

Also, by substituting (21) into (16), M_{DCM} is expressed as follows:

$$\begin{cases}M_{DCM}=\dfrac{d}{\sqrt{3k_{L(tot)}}}\\ k_{L(tot)}=\dfrac{2L_{tot}}{RT_S}\end{cases} \tag{22}$$



(a) (b)

Fig. 3 The operation principle of the recommended structure; a) basic waveforms of the presented structure in DCM and b) related circuit with mode 3.

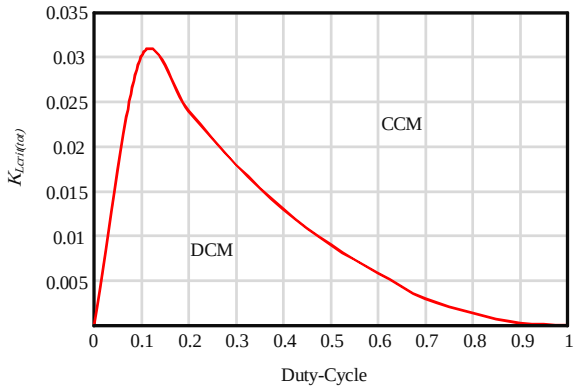


Fig. 4 The curve of $k_{Lcrit(tot)}$ versus the duty cycle (d).

2.3 Operation in Boundary Conduction Mode (BCM)

The $k_{L(tot)}$ curve versus duty cycle (d), which demonstrates the operation domain between the DCM operation and CCM operation, has been depicted in Fig. 4. That is apparent that the content of $k_{L(tot)}$ determines the operational area. Thus, when the $k_{L(tot)}$ is lower than the $k_{Lcrit(tot)}$, the presented converter will be worked in CCM. It should be noticed that the presented topology operates in BCM, when the voltage gain relation of the CCM (M_{CCM}) is equal to the voltage gain relation of the DCM (M_{DCM}). So, the $k_{Lcrit(tot)}$ can be calculated as follows:

$$K_{Lcrit\,(tot)} = \frac{(1-d)^2}{27} \tag{23}$$

3 Calculation of Peak Voltage on Semiconductors

According to Fig .2(c), the maximum voltage through the main switch can found as follows:

$$V_s = V_{in} + V_{C3} \rightarrow V_s = V_{in} + \frac{d}{1-d}V_{in} = \frac{1}{1-d}V_{in} = \frac{V_o}{3d} \tag{24}$$

The main switch is conducting and the diodes are reverse biased in the first mode, which is shown in Fig. 2(b). Hence, the maximum voltage stress of the diodes can be earned as follows:

$$V_{D1} = -V_{in} - V_{C1} \rightarrow$$

$$V_s = -V_{in} - V_{C3} = -V_{in} - \frac{d}{1-d}V_{in} = \frac{1}{1-d}V_{in} = -\frac{V_o}{3d} \tag{25}$$

$$V_{D2} = -V_{in} - V_{C4} \rightarrow$$

$$V_{D2} = -V_{in} - V_4 = -V_{in} - \frac{2d}{1-d}V_{in} = -\frac{1+d}{1-d}V_{in}$$

$$= -\frac{1+d}{3d}V_o \tag{26}$$

$$V_{Do} = V_{C1} - V_{in} - V_o \rightarrow$$

$$V_{Do} = \frac{2d}{1-d}V_{in} - V_{in} - \frac{3d}{1-d}V_{in} = -\frac{1+d}{1-d}V_{in}$$

$$= -\frac{1+d}{3d}V_o \tag{27}$$

From (9), the duty-cycle of the proposed converter is found as follows:

$$d = \frac{M_{CCM}}{M_{CCM}+3} \tag{28}$$

Regarding to (31), the normalized voltage stress throughout the switch (M_s) and diodes D_1 (M_{D1}), D_2 (M_{D2}), and D_o (M_{Do}) are determined in the following:

$$M_s = \frac{M_{CCM}+3}{3M_{CCM}} \tag{29}$$

$$M_{D1} = \frac{M_{CCM}+3}{3M_{CCM}} \tag{30}$$

$$M_{D2} = M_{Do} = \frac{4M_{CCM}+3}{3M_{CCM}} \tag{31}$$

From (29)–(31), it can be mentioned that the normalized voltage stress throughout the semiconductor elements is small compared to the output voltage, which

leads to decreasing power losses of the semiconductors.

4 Converter Efficiency Survey

The efficiency of the suggested topology can be expressed via the parasitic components of the suggested structure as follows:
$r_{DS\text{-}ON}$: power switch resistance in ON-state;
r_C: ESR values of capacitors;
r_D: diodes D_1, D_2, and D_o On-state resistance;
v_{FD}: forward voltage of diodes;
r_L: ESR value of the magnetic elements.

The following equation is utilized to estimate the efficiency of the suggested converter:

$$\eta = \frac{P_{out}}{P_{out} + \Delta P} \times 100\% \tag{32}$$

$$\Delta P = A_1 + A_2 + A_3 + A_4 + A_5 + A_6 \tag{33}$$

A_1 is the power losses of the switch, which includes switching losses ($P_{switching}$) and conduction losses ($P_{rDS\text{-}ON}$). The switch total losses equation is given in the following:

$$A_1 = P_{rDS-ON} + P_{switching} \rightarrow \begin{cases} P_{rDS-ON} = r_{DS-ON} i^2_{RMS,s} \\ P_{switching} = \frac{1}{2} f_s (t_r + t_f) I_{sw} V_s \end{cases} \tag{34}$$

A_2 is the magnetic losses of the suggested structure which is defined as follows:

$$A_2 = r_{L1} i^2_{L1,RMS} + r_{L2} i^2_{L2,RMS} + r_{L3} i^2_{L3,RMS} \tag{35}$$

The power losses of diodes which consist of forward voltage losses of diodes (P_{FD}) and conduction losses of diodes (P_{Con}) are named with A_3. The following equation is utilized for calculating the power losses of diodes:

$$A_3 = P_{Con} + P_{FD} \rightarrow \begin{cases} P_{Con} = r_{Diodes} i^2_{RMS,Diodes} \\ P_{FD} = V_{F(Diodes)} I_{(avg)Diodes} \end{cases} \tag{36}$$

The power losses of the capacitors (A_4) are obtained as follows:

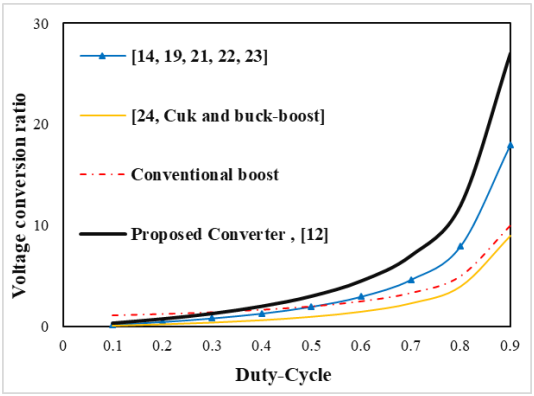
$$A_4 = r_{C1} i^2_{C1,RMS} + r_{C2} i^2_{C2,RMS} + r_{C3} i^2_{C3,RMS} + r_{C4} i^2_{C4,RMS} + r_{Co} i^2_{Co,RMS} \tag{37}$$

5 Comparison Survey

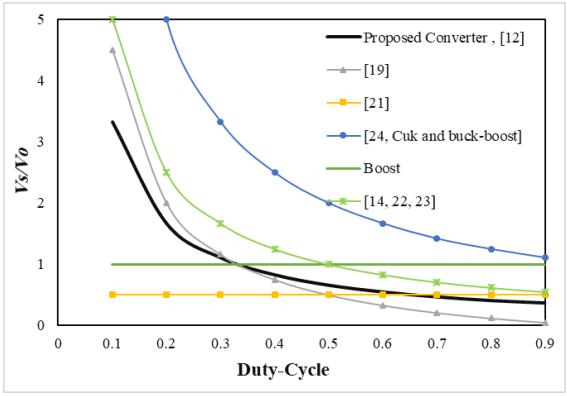
In this section, the proposed structure is compared with some buck-boost converters in terms of the voltage conversion ratio, peak voltage through the switch and the number of elements. Table 1 illustrates the comparison specifications of the suggested converter and other works. It has to be mentioned that in Table 1, all efficiencies are calculated with about the same power level. The maximum efficiency is considered for the conventional buck-boost converter. As seen in Figs. 5(a) and 5(b), it is obvious that the condition such as duty-cycle in all converter is the same. Also, the proposed topology is compared with topologies in the same family of buck-boost converters with the same structures. The curve of the voltage gain versus duty-cycle is demonstrated in Fig. 5(a). Related to this figure, the proposed converter can provide a high voltage rate in comparison with conventional boost, buck-boost, CUK, the mentioned converter in [19], and the converter in [21]. It has to be noticed that the recommended structure voltage conversion ratio is increased by raising the duty-cycle. The peak voltage through the switch of the suggested converter and other topologies has been indicated in Fig. 5(b). Related to Fig. 5(b), that is clear that the maximum voltage through the switch of the suggested structure is lower than the other topologies. In addition, the proposed structure utilizes one power switch. Thus, the conduction losses of the recommended topology can be decreased, and finally, the overall system efficiency can be increased. The voltage gain and the maximum voltage across the switch of the recommended converter is equal to the [12]. However, there is no soft-switching capability in [12] and also the efficiency of the suggested converter is high compared to the converter [12]. Although the presented converter utilizes more

Table 1 Comparison specification of suggested topology and the other buck-boost topologies.

Converter	[12]	[14]	[19]	[21]	[22]	[23]	[24]	Cuk	Conventional buck-boost	Proposed converter
M_{CCM}	$\frac{3d}{1-d}$	$\frac{2d}{1-d}$	$\frac{2d}{1-d}$	$\frac{2d}{1-d}$	$\frac{2d}{1-d}$	$\frac{2d}{1-d}$	$\frac{d}{1-d}$	$\frac{d}{1-d}$	$\frac{d}{1-d}$	$\frac{3d}{1-d}$
Voltage stress of switch	$\frac{V_o}{3d}$	$\frac{V_o}{2d}$	$\frac{1-d}{2d}V_o$	$\frac{V_o}{2}$	$\frac{V_o}{2d}$	$\frac{V_o}{2d}$	$\frac{V_o}{d}$	$\frac{V_o}{d}$	$\frac{V_o}{d}$	$\frac{V_o}{3d}$
No. of switches	1	1	3	1	1	1	2	1	1	1
No. of diodes	3	2	3	2	2	2	2	1	1	3
No. of capacitors	5	3	1	3	4	4	2	2	1	6
No. of inductors	3	2	2	2	3	3	2	2	1	4
Soft switching	No	No	No	No	No	No	No	-	-	Yes
Efficiency [%]	95.9	94.2	97	93.2	95.3	95.2	95.1	-	-	96.1



(a)



(b)

Fig. 5 The comparison results of the proposed converter with other buck-boost converters; a) M_{CCM} and b) The peak voltage through the switch.

Table 2 Component specification of the recommended structure.

Parameter	Step-up mode	Step-down mode
Input-voltage (V_{in})	20 V	40 V
Output-voltage (V_{out})	90 V	30 V
Output power (P_{out})	100 W	50 W
Frequency (f_s)	50 kHz	50 kHz
Duty-cycle (d)	0.6	0.2
Selected devices		
Capacitors C_1, C_2, C_3, C_4, and C_B	220V/200 µF	
Diode D_1, D_2, and D_o	MUR1016	
Switch (S)	IRFP260N	
Capacitor C_o	450V/1500 µF	
Inductor L_1	Ferric core (500 µH)	
Inductor L_2, L_3, and L_B	Ferric core (600 µH)	

number of components, however, it has a larger output voltage rate and less voltage stress on the main switch in comparison with other topologies. The converters mentioned in [14] and [22-24] has can produce low voltage rates with high losses and higher peak voltage compared to the suggested converter. Besides, the soft-switching condition does not exist in the introduced converters of Table 1, So the power losses will be high in these converters. By demonstrating the advantages and drawbacks of the proposed structure, it can be concluded that the recommended converter can be applied in various power levels for instant sustainable energy, LED drivers, etc.

6 Experimental Test Results

In order to show the proficiency of the suggested converter, the experimental prototype has been implemented and tested in the laboratory. The basic characteristics of the proposed converter are illustrated in Table 2. It has to be mentioned that the experimental results are given for both step-up and step-down switching states.

Step-up mode: The experimental measurement results of the proposed converter in step-up mode are demonstrated in Figs. 6-8. The voltage and current waveforms through the main switch and diodes D_1, D_2, and D_o are demonstrated in Figs. 6(a)-(d), respectively. Fig. 6(a) indicates the voltage and current waveforms of the main switch which are about 49V and 9A, respectively. It has to be noticed that the peak voltage through the switch is smaller than the output voltage, which decreases the conduction loss of the switch. The voltage and current values of the diode D_1 are about 48V and 2.3A which is illustrated in Fig. 6(b). The peak voltage and the peak current through the diode D_2 are indicated in Fig. 6(c) which are almost 48V and 2.8A. The maximum voltage across the diode D_o is the same as the diodes D_1 and D_2, and equals to 48V and also, the peak current of diode D_o is 2.8A. The waveforms of voltages across the capacitors C_1, C_2, C_3, and C_o are illustrated in Figs. 7(a)-(d), respectively. As indicated in this figure, voltages V_{C1} and V_{C4} are equal to 58V, and voltages V_{C2} and V_{C3} are equal to 29V. These capacitors voltages verify the obtained voltages equations in (9) and (10). The waveforms of inductors L_1, L_2, and L_3 currents and the output voltage are indicated in Figs. 8(a)-(d), respectively. As depicted in Figs. 8(a)-(c), the ripple contents of the inductor currents are acceptable for DC-DC converters. The output voltage waveform is illustrated in Fig. 8(d), which is about 90V. It is noticed that the voltage ripple through the output voltage is poor and it can be ignored.

Step-down mode: The experimental measurement results of the suggested structure operation in step-down

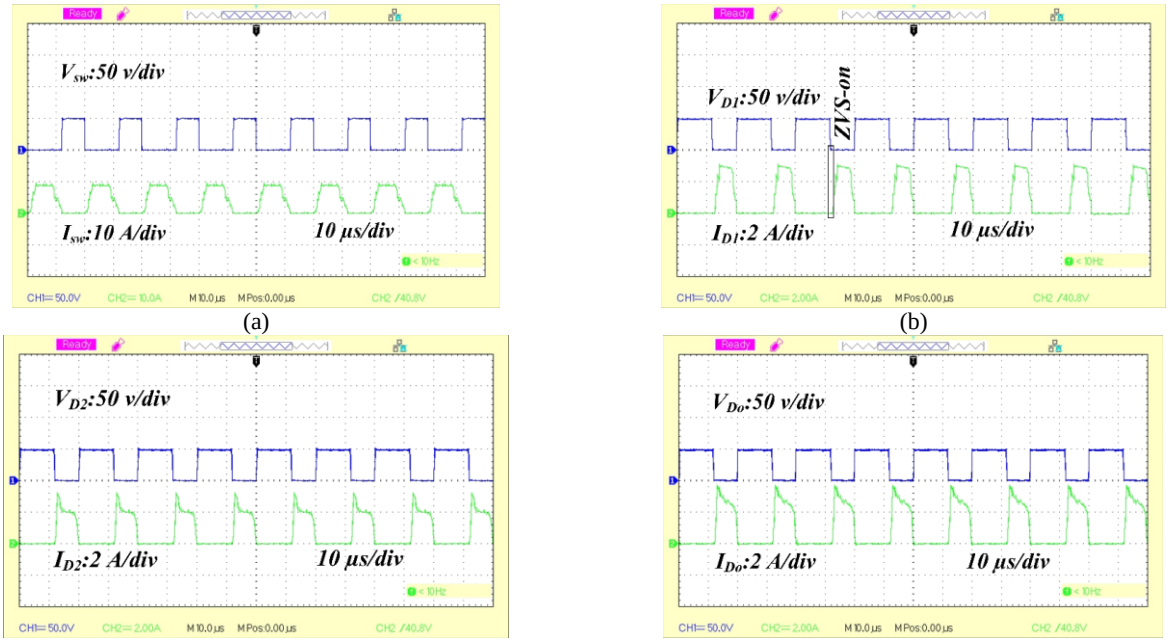


Fig. 6 The measured voltages and currents; a) V_{sw}-I_{sw}, b) V_{D1}-I_{D1}, c) V_{D2}-I_{D2}, and d) V_{Do}-I_{Do}.

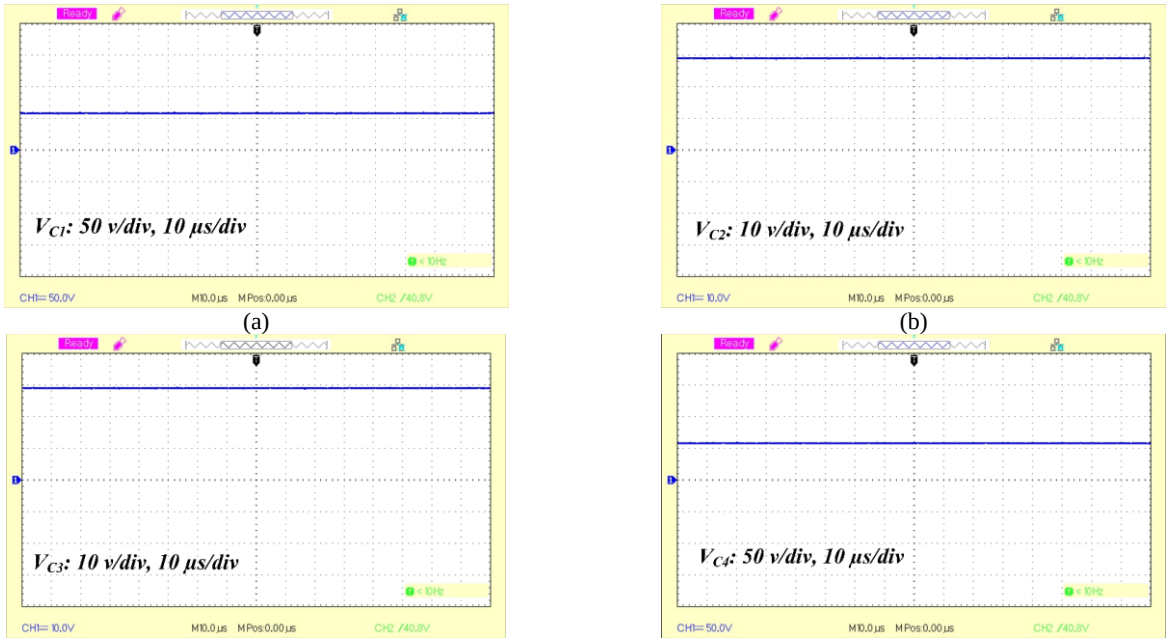


Fig. 7 The measured voltages; a) V_{C1}, b) V_{C2}, c) V_{C3}, and d) V_{C4}.

mode are illustrated in Figs. 9-11. Fig. 9(a) indicates the voltage and current waveforms of the main switch which are about 49V and 3.2A. The diode D_1 voltage and current, V_{D1} and i_{D1}, are equal to 49V and 1.3A, which are indicated in Fig. 9(b). As given in Fig. 9(c), the maximum voltage and maximum current of diode D_2 are about 49V and 1.2A. The current and voltage waveforms of the diode D_o are demonstrated in Fig. 9(d). The peak voltage and peak current through diode D_o are equal to 49V and 1.2A. The capacitors C_1, C_2, C_3, and C_4 voltage waveforms are depicted in Figs. 10(a)-(d), respectively as V_{C1} and V_{C4} are equal to 19V, and V_{C2} and V_{C3} are equal to 19V. The inductors L_1, L_2, and L_3 current waveforms are illustrated in Figs. 11(a)-(c), respectively. As indicated in this figure, the ripple contents of inductors current in buck mode are acceptable for DC-DC structures as same as the boost mode. The output voltage waveform is shown in Fig. 11(d) which is about 29V with poor voltage ripple value.

The recorded efficiencies of the suggested converter in both step-up and step-down switching states for

different output power levels are indicated in Figs. 12(a)-(b). Moreover, the power losses diagrams of the recommended converter based on the obtained equations in the efficiency survey for both step-up and step-down modes are depicted in Figs. 12(c)-(d). As illustrated in Figs. 12(a)-(b), the maximum efficiency of the suggested converter in step-up mode is equal to 95.9% and in step-down mode is equal to 95.3%. According to Figs. 12(a)-(b), the efficiency tolerance of the suggested converter is relatively low.

Concerning theoretical survey and laboratory results, it can be mentioned that the suggested structure can be an acceptable choice for renewable energies for instant PV panels because of high efficiency with lower maximum voltage throughout the semiconductors.

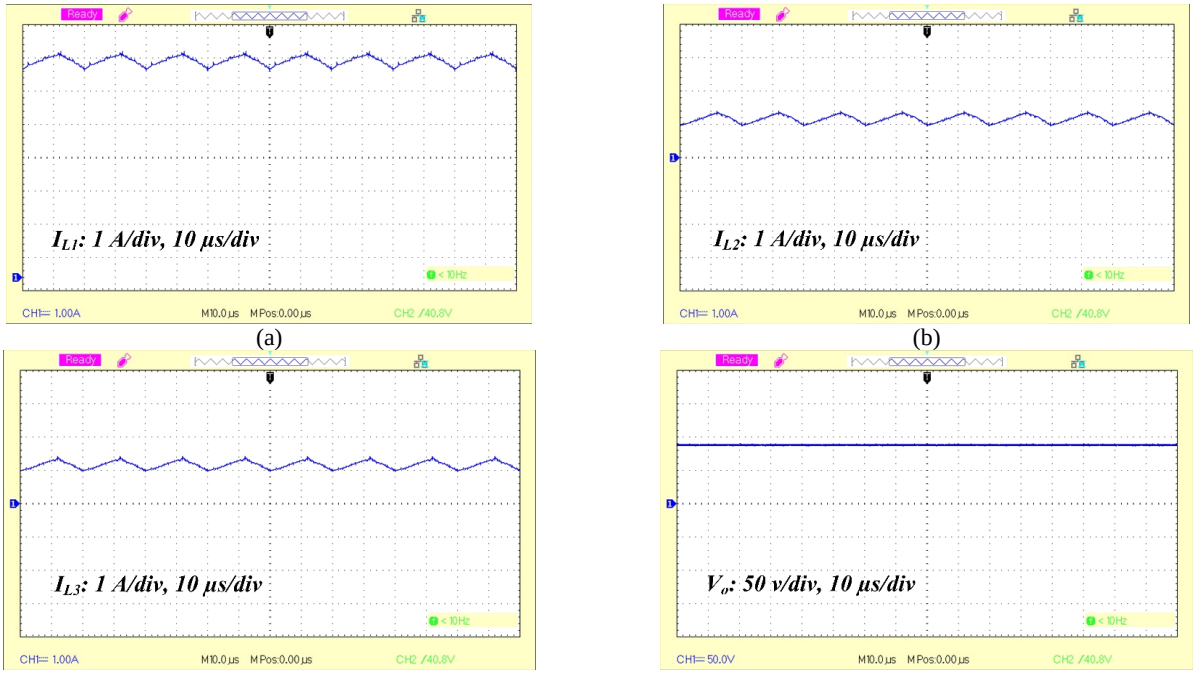


Fig. 8 The measured voltages and currents; a) i_{L1}, b) i_{L2}, c) i_{L3}, and d) V_{out}.

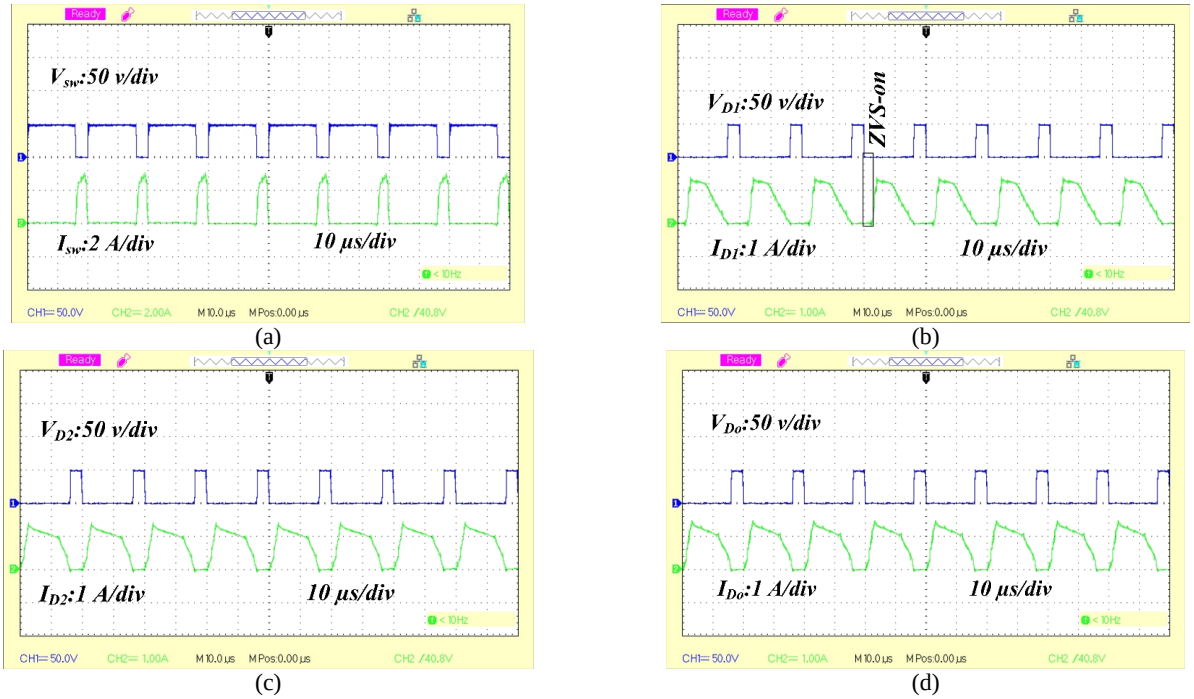


Fig. 9 The measured voltages and currents; a) V_{sw}-I_{sw}, b) V_{D1}-I_{D1}, c) V_{D2}-I_{D2}, and d) V_{Do}-I_{Do}.

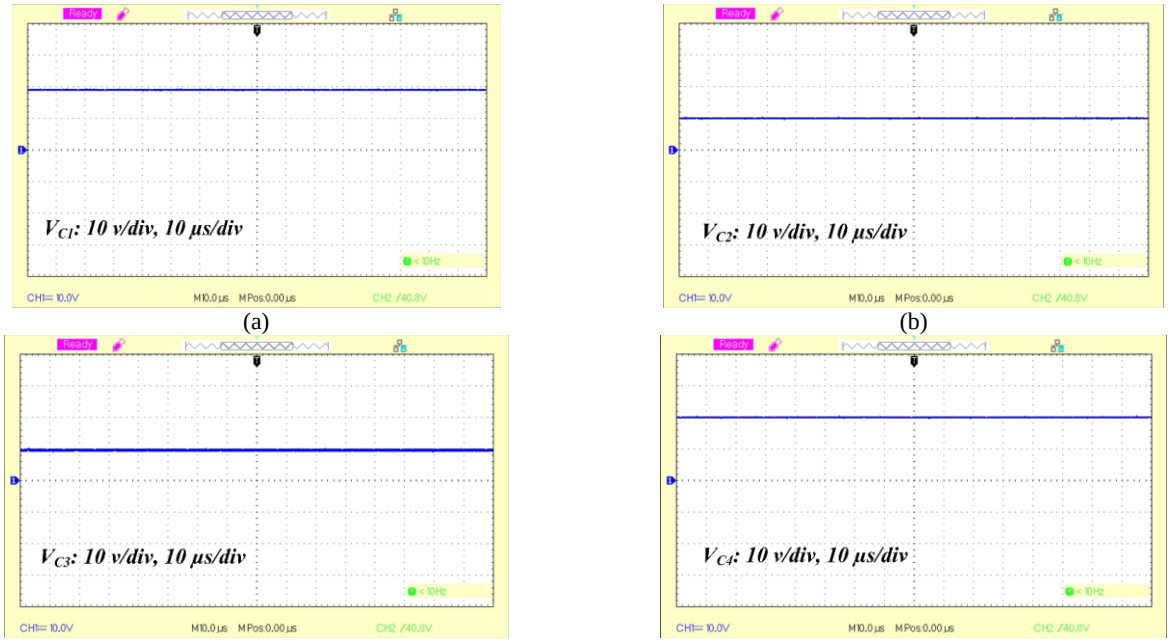


Fig. 10 The measured voltages; a) V_{C1}, b) V_{C2}, c) V_{C3}, and d) V_{C4}.

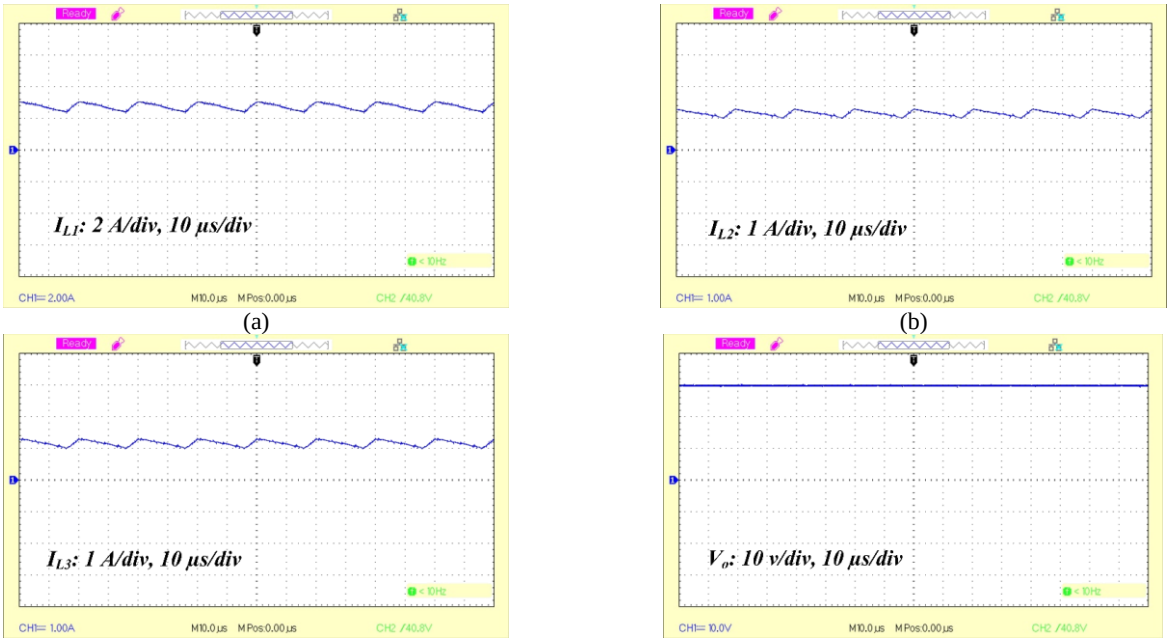


Fig. 11 The measured voltage and currents; a) i_{L1}, b) i_{L2}, c) i_{L3}, and d) V_{out}.

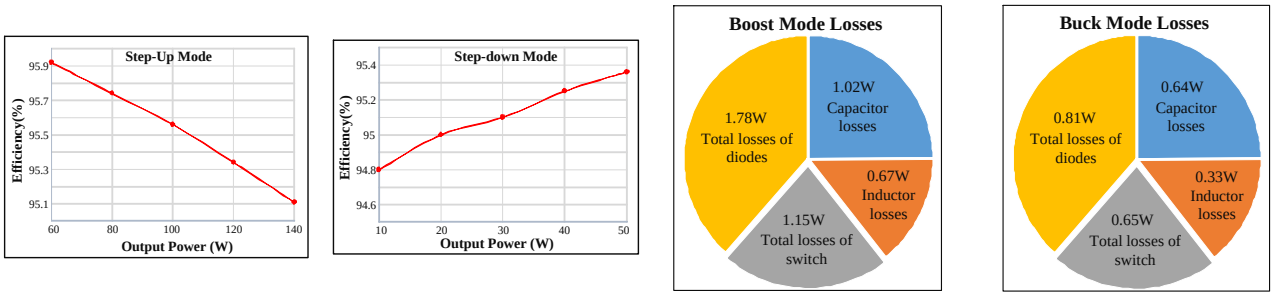


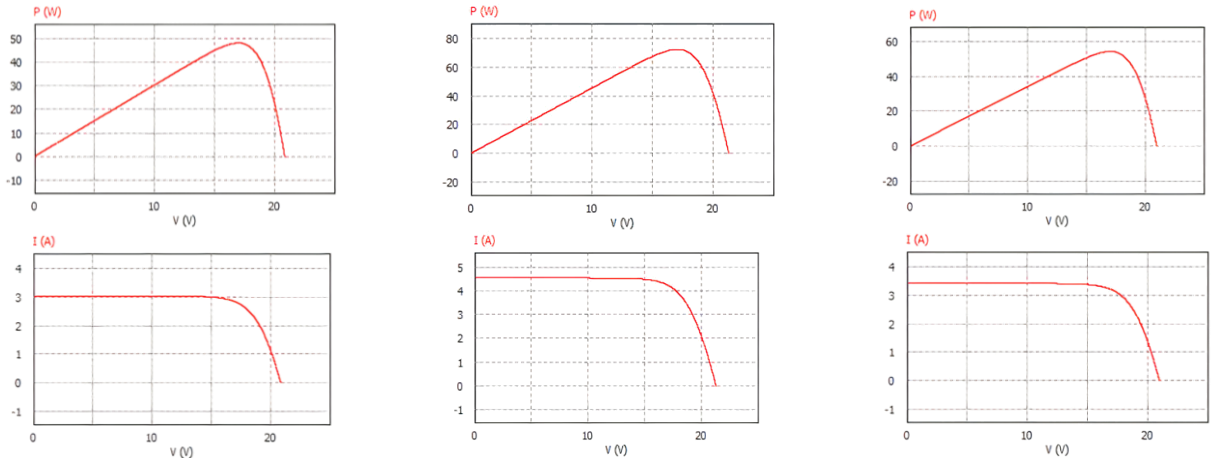
Fig. 12 Efficiency and losses curves a) boost efficiency, b) buck efficiency, c) boost losses, and d) buck losses.

6.1 Simulation Results of MPPT Implementation in the Proposed Converter

In order to demonstrate the proficiency of the suggested converter, the MPPT capability of the proposed structure is indicated by simulation results for step-up mode. The PV module that is used to simulate the PV solar system, is the physical type available in PSIM software. The full specifications of the used PV module have been demonstrated in Table 3. Perturb & Observe (P&O) algorithm is utilized to extract the maximum power point (MPPT) from the PV system [25]. In order to properly investigate the effect of changing the environmental factors (temperature and intensity of irradiance), only the effect of one factor is investigated while the other factor has considered constant. Generally, changing the intensity of irradiance has a high impact on the changing of the MPPT point. Therefore, in this section, the temperature of the PV module is kept constant at 25˚C, and MPPT is tested only in variable irradiance intensity. The P-V and I-V curves of the PV module at different radiations such as 800 W/m^2, 1200 W/m^2, and 900 W/m^2 have been shown in Figs. 13(a)-(c), respectively. Figs. 14(a)-(f) indicates the simulation results of the MPPT implementation at the proposed structure for the different irradiations. As depicted in Fig. 14, the obtained maximum power and its corresponding voltage are very close to the maximum power point of the P-V scheme in the PV module. As a result, the utilized MPPT algorithm at the suggested structure has acceptable performance.

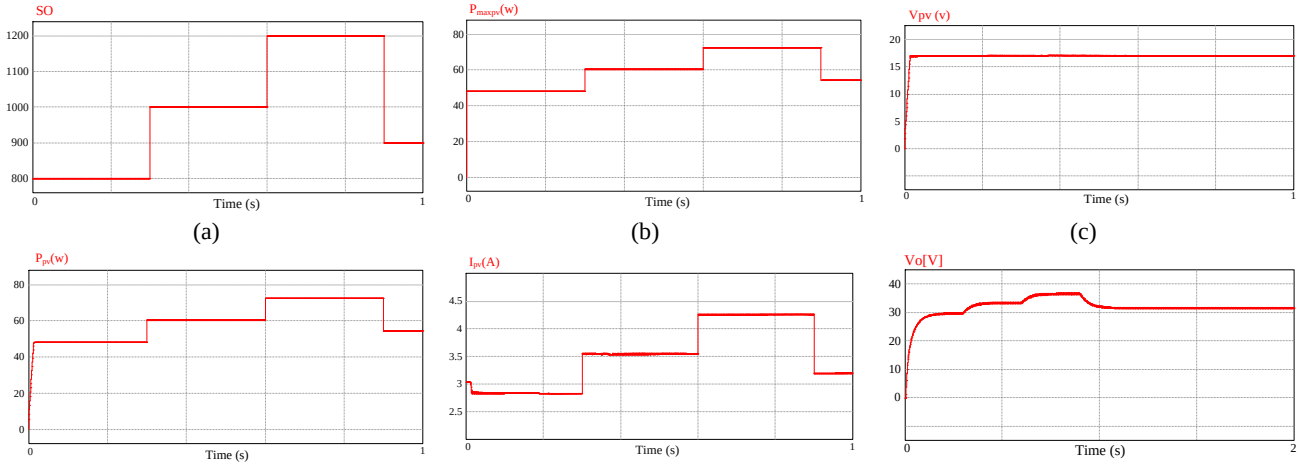
Table 3 The specifications of the used PV module in PSIM software.

Parameter	Value
Number of cells (N_s)	36
Maximum power (P_{max})	60 W
Voltage at P_{max}	17.1 V
Current at P_{max}	3.5 A
Open circuit voltage (V_{oc})	21.1 V
Short circuit current (I_{sc})	3.8A



(a) (b) (c)

Fig. 13 P-V and I-V curves of the PV module at different radiations; a) 800 W/ m^2, b) 1200 W/m^2, and c) 900 W/m^2.



(a) (b) (c)

(d) (e) (f)

Fig. 14 The simulation results of the MPPT algorithm; a) radiation intensity changing, b) maximum power of PV under different radiation, c) V_{PV}, d) P_{PV}, e) I_{PV}, and f) output voltage of the proposed converter.

In the first irradiation pattern (G=800 W/m^2), the obtained output power (P_{PV}) of the PV panel is equal to 48.29W. Also, P_{max} of the P-V curve is 48.30W. Thus, the MPPT efficiency for the first irradiation pattern is calculated as follows:

$$\eta_{MPPT\ (800\ w/m^2)} = \frac{P_{PV}}{P_{\max}} \times 100 = \frac{48.29}{48.30} \times 100\% = 99.97\% \quad (38)$$

Moreover, the MPPT efficiency for irradiation 1200 W/m^2 and 900 W/m^2 are obtained as follows:

$$\eta_{MPPT\ (1200\ w/m^2)} = \frac{P_{PV}}{P_{\max}} \times 100 = \frac{72.63}{72.64} \times 100\% = 99.98\% \quad (39)$$

$$\eta_{MPPT\ (900\ w/m^2)} = \frac{P_{PV}}{P_{\max}} \times 100 = \frac{54.42}{54.43} \times 100\% = 99.98\% \quad (40)$$

6.2 Dynamic Behavior of the Recommended Converter

The state-space average method can be utilized for indicating the dynamic behavior of the suggested structure. The following variables and equations are given as the state, input, and control variable subordinate [26]:

$$\begin{aligned} \hat{x}_i'(t) &= A\hat{x}_i(t) + B\hat{u}_i(t) \\ \hat{y}_i(t) &= C\hat{x}_i(t) + D\hat{u}_i(t) \end{aligned} \quad (41)$$

To calculate the state equations some presumptions are remarked as follows:

- The ESR value of all components is not considered;
- The input source has a continuous current.

It has to be defined that the state variables vector is $\hat{x}_i'(t)$, the input variables vector is $(\hat{u}_i(t))$ and the output variables are $\hat{y}_i(t)$, which has been expressed as follow:

$$\hat{x} = [\hat{i}_{L1}, \hat{i}_{L2}, \hat{i}_{L3}, \hat{i}_{LB}, \hat{v}_{C1}, \hat{v}_{C2}, \hat{v}_{C3}, \hat{v}_{C4}, \hat{v}_{CB}, \hat{v}_{Co}]^T \quad (42)$$

$$\hat{u} = [\hat{v}_{in}, \hat{i}_o, \hat{i}_{D2}, \hat{i}_{Do}, \hat{d}]^T \quad (43)$$

$$\hat{y} = [\hat{i}_{in}, \hat{v}_o]^T \quad (44)$$

The equations related to the state and output variables can be achieved as follows by using Kirchhoff's voltage and current principles:

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \frac{d-1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_2} & \frac{d-1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{d+1}{L_3} & 0 & 0 & \frac{1}{L_3} & 0 & \frac{d-1}{L_3} \\ 0 & 0 & 0 & 0 & -\frac{1}{L_B} & \frac{1-d}{L_B} & 0 & \frac{d-1}{L_B} & \frac{d}{L_B} & \frac{1-d}{L_B} \\ 0 & 0 & \frac{d}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1-d}{C_3} & -\frac{d}{C_3} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1-d}{C_4} & 0 & -\frac{d}{C_4} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (45)$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & \frac{V_{in}}{L_1} \\ \frac{1}{L_2} & 0 & 0 & 0 & \frac{V_{in}}{L_2} \\ \frac{1}{L_3} & 0 & 0 & 0 & \frac{V_{in}}{L_3} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_1} & \frac{I_{L3}+I_{Do}}{C_1} \\ 0 & 0 & \frac{1-d}{C_2} & 0 & -\frac{I_{D2}}{C_2} \\ 0 & \frac{1-d}{C_3} & 0 & 0 & -\frac{I_o+I_{L1}+I_{L2}}{C_3} \\ 0 & \frac{1-d}{C_4} & 0 & 0 & -\frac{I_o+I_{L1}+I_{L3}}{C_4} \\ 0 & 0 & 0 & \frac{1}{C_B} & \frac{I_{Do}}{C_B} \\ 0 & -\frac{1}{C_o} & 0 & \frac{d}{C_o} & \frac{I_{Do}}{C_o} \end{bmatrix} \quad (46)$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad (47)$$

The open-loop transfer function and Bode diagram are utilized for recognizing the dynamic behavior of the recommended structure. The transfer function of the control to the output (the magnitude dB and phase frequency response) in the Laplace area, which is defined as a Bode diagram is illustrated in Fig. 15(a). The load voltage can be controlled by using the closed-loop scheme with a PI controller that is depicted in Fig. 15(b). As depicted in Fig. 15(b), the appropriate content of the produced voltage ($V_{o,Ref}$) is compared with V_o. The differences between the V_o and $V_{o,Ref}$ are transferred. Then, the PI controller produces a suitable duty-cycle. The produced duty-ratio and carrier wave are compared to each other to provide accurate interpolated. It should be mentioned that the content of PI controller variables, which includes a gain and time constant can be obtained by a try and error method.

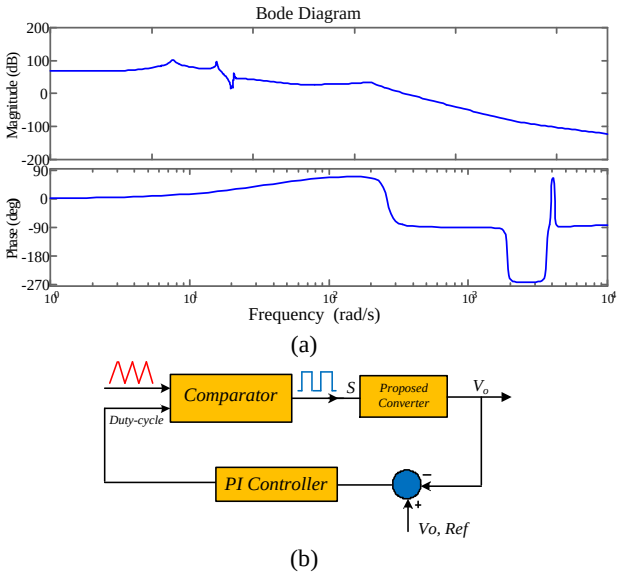


Fig. 15 Dynamic response of the suggested converter; a) Bode diagram of control to output transfer function and b) closed loop control of the suggested.

7 Conclusions

In this study, a transformer-less buck-boost converter with a high voltage conversion ratio was proposed. The introduced structure can be categorized as 1) high voltage conversion ratio in both step-up and step-down switching state, 2) lower peak voltage through the semiconductors by using an interleaved configuration, 3) high efficiency and 4) low reverse recovery losses because of the existence of soft-switching condition such a ZVS. In addition, in the dynamic response section, it has been shown that the control of the circuit is simple because of using only one power switch. To indicate the effectiveness of the recommended structure a technical survey such as mode analysis is carried out. With regard to the comparison section, it has been shown that the suggested structure has high voltage gain with high efficiency, a low number of components and soft-switching capability among the other previous works. Finally, laboratory test results for DC voltage source 20V and load voltage 90V with full load efficiency of 95.1% for step-up mode and also laboratory test results for DC voltage source 40V and load voltage 30V with full load efficiency of 95.37% for step-down mode were provided to indicates the proficiency of the recommended structure. Moreover, it has been demonstrated that the presented converter has MPPT capability, which makes it to utilize in renewable energy systems. According to the presented converter characteristics, it can be an appropriate choice in power conversion systems for instant sustainable energy systems, hybrid electric vehicles, LED drivers, etc.

References

[1] S. Pourjafar, F Sedaghati, H. Shayeghi, and M. Maalandish, "High step-up DC–DC converter with coupled inductor suitable for renewable applications," *IET Power Electronics*, Vol. 12, No. 1, pp. 92–101, Oct. 2018.

[2] M. Maalandish, S. Pourjafar, S. H. Hosseini, and N. Taghizadegan. "Leakage current elimination with improved non-isolated nine-level inverter for grid-connected PV panels," *Journal of Energy Management and Technology*, Vol. 1, No. 2, pp. 46–55, Oct. 2017.

[3] F. Sedaghati and S. Pourjafar, "Analysis and implementation of a boost DC–DC converter with high voltage gain and continuous input current," *IET Power Electronics*, Vol. 13, No. 4, pp. 798–807, Nov. 2019.

[4] H. S. Son, J. K. Kim, J. B. Lee, S. S. Moon, J. H. Park, and S. H. Lee, "A new buck-boost converter with low-voltage stress and reduced conducting components," *IEEE Transactions on Industrial Electronics*, Vol. 64, No. 9, pp. 7030–7038, Mar. 2017.

[5] S. Siouane, S. Jovanović, and P. Poure, "Service continuity of PV synchronous buck-buck-boost converter with energy storage," *Energies*, Vol. 11, No. 6, p.1369, Jun. 2018.

[6] S. Pourjafar, H. Shayeghi, H. Madadi Kojabadi, M. Maalandish, and F. Sedaghati, "A coupled inductor based high voltage gain DC-DC converter using interleaved voltage multiplier cells," *Iranian Journal of Electrical and Electronic Engineering*, Vol. 16, No. 1, pp. 1–12, Mar. 2020.

[7] E. Babaei and T. Ahmadzadeh, "A new structure of buck-boost Z-source converter based on ZH converter," *Journal of Operation and Automation in Power Engineering*, Vol. 4, No. 2, pp. 117–131, Dec. 2016.

[8] M. Amiri and H. Farzanehfard, "A high-efficiency interleaved ultra-high step-down DC–DC converter with very low output current ripple," *IEEE Transactions on Industrial Electronics*, Vol. 66, No. 7, pp. 5177–5185, Sep. 2018.

[9] Z. Zhou, H. Li, and X. Wu, "A constant frequency ZVS control system for the four-switch buck-boost DC–DC converter with reduced inductor current," *IEEE Transactions on Power Electronics*, Vol. 34, No. 7, pp. 5996–6003, Dec. 2018.

[10] J. You, W. Fan, L. Yu, B. Fu, and M. Liao, "Disturbance rejection control method of double-switch buck-boost converter using combined control strategy," *Energies*, Vol. 12, No. 2, p. 278, Jan. 2019.

[11] K. I. Hwu and T. J. Peng, "A novel buck-boost converter combining KY and buck converters," *IEEE Transactions on Power Electronics*, Vol. 27, No. 5, pp. 2236–2241, Dec. 2011.

[12] M. R. Banaei and H. A. F. Bonab, "A novel structure for single-switch non-isolated transformer-less buck-boost DC–DC converter," *IEEE Transactions on Industrial Electronics*, Vol. 64, No. 1, pp. 198–205, Sep. 2016.

[13] C. L. Shen and P. C. Chiu, "Buck-boost-Flyback integrated converter with single switch to achieve high voltage gain for PV or fuel-cell applications," *IET Power Electronics*, Vol. 9, No. 6, pp. 1228-1237, May. 2016.

[14] B. Zhu, S. Hu, G. Liu, Y. Huang, and X. She, "Low-voltage stress buck-boost converter with a high voltage conversion gain," *IEEE Access*, Vol. 8, pp. 95138–95196, May. 2020.

[15] A. Villarruel-Parra and A. J. Forsyth, "Modeling phase interactions in the dual-interleaved buck converter using sampler decomposition," *IEEE Transactions on Industrial Electronics*, Vol. 66, No. 5, pp. 3316–3322, Jul. 2019.

[16] H. Wu, T. Mu, H. Ge, and Y. Xing, "Full-range soft-switching-isolated buck-boost converters with integrated interleaved boost converter and phase-shifted control," *IEEE Transactions on Power Electronics*, Vol. 31, No. 2, pp. 987–999, Apr. 2015.

[17] J. M. Blanes, R. Gutiérrez, A. Garrigós, J. L. Lizán, and J. M. Cuadrado, "Electric vehicle battery life extension using ultracapacitors and an FPGA controlled interleaved buck-boost converter," *IEEE Transactions on Power Electronics*, Vol. 28, No. 12, pp. 5940–5948, Mar. 2015.

[18] E. Babaei, Z. Saadatizadeh, and B. M. Ivatloo, "A new interleaved bidirectional zero voltage switching DC-DC converter with high conversion ratio," *Journal of Circuits, Systems and Computers*, Vol. 26, No. 06, p. 1750105, Jun. 2017.

[19] H. K. Liao, T. J. Liang, L. S Yang, and J. F. Chen, "Non-inverting buck-boost converter with interleaved technique for fuel-cell system," *IET Power Electronics*, Vol. 5, No. 8, pp. 1379–1388, Sep. 2012.

[20] J. C. Rosas-Caro, J. E. Valdez-Resendiz, J. C. Mayo-Maldonado, A. Alejo-Reyes, and A. Valderrabano-Gonzalez, "Quadratic buck-boost converter with positive output voltage and minimum ripple point design," *IET Power Electronics*, Vol. 11, No. 7, pp. 1306–1313, Mar. 2018.

[21] M. R. Banaei, H. Ardi, and A. Farakhor, "Analysis and implementation of a new single-switch buck-boost DC/DC converter," *IET Power Electronics*, Vol. 7, No. 7, pp. 1906–1914, May. 2014.

[22] M. R. Banaei and H. A. F. Bonab, "A high efficiency non-isolated buck-boost converter based on zeta converter," *IEEE Transactions on Industrial Electronics*, Vol. 67, No. 3, pp. 1991–1998, Mar. 2019.

[23] M. R Banaei, H. A. F. Faeghi Bonab, and N. Taghizadegan Kalantari, "Analysis and design of a new single switch non-isolated buck-boost DC-DC converter," *Journal of Operation and Automation in Power Engineering*, Vol. 8, No. 2, pp.116–127, Aug. 2020.

[24] M. Veerachary and V. Khubchandani, "Analysis, design, and control of switching capacitor based buck-boost converter," *IEEE Transactions on Industry Applications*, Vol. 55, No. 3, pp. 2845–2857, Dec. 2018.

[25] M. A. Ramli, S. Twaha, K. Ishaque, and Y. A. Al-Turki, "A review on maximum power point tracking for photovoltaic systems with and without shading conditions," *Renewable and Sustainable Energy Review*, Vol. 67, pp. 144–159, 2017,

[26] T. Suntio, T. Messo, and J. Puukko, *Power electronic converters: dynamics and control in conventional and renewable energy applications*. John Wiley & Sons, Wiley-VCH Verlag GmbH & Co. KGaA, Boschstr.12, 69469 Weinheim, Germany.

H. Shayeghi received the B.Sc. And M.S.E. Degrees in Electrical and Control Engineering in 1996 and 1998, respectively, and the Ph.D. degree in Electrical Engineering from Iran University of Science and Technology (IUST), Tehran, Iran, in 2006. Currently, he is a Full Professor in the Technical Engineering Department of the University of Mohaghegh Ardabili, Ardabil, Iran. His research interests are in the application of robust control, artificial intelligence, and heuristic optimization methods to power system control design, operation, and planning, power system restructuring, and renewable energies applications. He has more than 320 papers in international journals and conference proceedings.

S. Pourjafar was born in May 1993 in Ardabil, Iran. He received his B.Sc. degree in Electrical Engineering from Azerbaijan Shahid Madani University, Tabriz, Iran, in 2015. He also received his M.Sc. in Power Electronics and Drives from the Sahand University of Technology, Faculty of Electrical and Computer Engineering, Tabriz, in 2017. He is currently a Ph.D. Candidate at the Electrical Engineering Department, University of Mohaghegh Ardabili. His research interests include DC-DC converters, inverters, application of power electronics in energy conversion systems (wind energy, solar energy, grid-connected inverters), battery charging applications in electric vehicles.

F. Sedaghati was born in Ardabil, Iran, in 1984. He received the M.Sc. and Ph.D. degrees both in Electrical Engineering in 2010 and 2014 from the University of Tabriz, Tabriz, Iran. In 2014, he joined the Faculty of Engineering, Mohaghegh Ardabili, where he has been an Assistant Professor since 2014. His current research interests include renewable energies and power electronic converters design and applications.