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Research Paper

Design of Gate-Driven Quasi Floating Bulk OTA-Based Gm–C Filter for PLL Applications

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Abstract: The advancement in the integrated circuit design has developed the demand for low voltage portable analog devices in the market. This demand has increased the requirement of the low-power RF transceiver. A low-power phase lock loop (PLL) is always desirable to fulfill the need for a low power RF transceiver. This paper deals with the designing of the low power transconductance- capacitance (G_m-C) based loop filter with the help of the gate-driven quasi bloating Bulk (GD-QFB) MOS technique. The GD-QFB MOS-based operational transconductance amplifier (OTA) has been proposed with a high dc gain of 82.41 dB and less power consumption of 188.72 µW. Further, G_m-C based active filter has been designed with the help of the proposed GD-QFB OTA. The simulation results of G_m-C filter attain a -3 dB cut-off frequency of 59.08 MHz and power consumption of 188.31µW at the supply voltage of 1V. The proposed G_m-C filter is suitable for the designing of 1-3 GHz low power PLL.

Keywords: Bulk Driven MOS, CMOS, Current Buffer Compensation, Gate Driven-Quasi Floating Bulk MOSFET, Phase Lock Loop.

1 Introduction

THE recent market requirement has increased the huge demand for portable electronic devices. This demand has reduced the size of modern CMOS technology [1-5]. To fulfill the demand of the market, integrated circuit design is adopting the low voltage circuit design approach such as bulk driven (BD) [3], quasi floating gate (QFG) MOS [4], dynamic threshold (DT) MOS [5], quasi floating bulk (QFB) MOS [6], etc. Phase lock loop (PLL) frequency synthesizer is one of the essential building blocks of the RF transceiver [7-9]. For the low power RF subsystem design, the requirement of a low-power phase lock loop is increased [9]. Low-voltage PLL's are used for the design of the system on chip (SOC) applications that is the main concern of the research. The main building blocks of the PLL are a phase detector, loop filter, voltage control oscillator (VCO), and frequency divider. The loop filter is one of the major building blocks that define loop stability that means how fast the loop achieves lock [8]. Another requirement of a loop filter is to control the reference spurs that appear at the phase detector output [9]. These reference spurs appear at VCO control input. There are many spur reduction techniques available in the literature [8, 9]. There is always a requirement of the careful design of the loop filter for low power PLL. To fulfill this demand, it is always required to design a low power loop filter. Passive loop filters are available in the literature for low power PLL design [7-10]. For a wide band PLL requirement, the increase in passive loop filter capacitor will increase the die area of PLL [7-11]. To overcome the limitations of the passive filter in wideband PLL, a G_m-C approach based low power active loop filter is proposed in this paper. G_m-C based active loop filter advantages over passive RC filter that provides the automatic tuning facility to the loop filter of PLL. The operational transconductance amplifier (OTA) is preferred as a basic building block of the G_m-C filter because of the automatic tuning facility by adjusting the transconductance of the OTA with the help of adjusting bias current (I_{bias}) as represented in Fig. 1.

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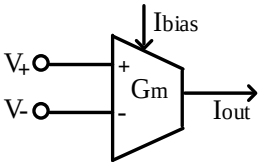

Fig. 1 OTA basic symbol.

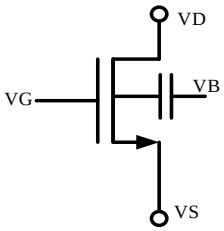

Fig. 2 N-channel GD-QFB MOSFET [6].

The output of the OTA is given as

$$I_{out} = G_m (V_+ - V_-) \quad (1)$$

The required transconductance for the G_m-C filter is designed with the help of OTA. In this paper, GD-QFB MOSFET based low power design technique is incorporated at the input of the differential stage OTA to achieve the low power operation.

The organization of the paper is as follows. Section 2 describes the GD-QFB MOS technique. Sections 3 and 4 deals with the designing of gate-driven OTA and proposed GD-QFB input based current compensated OTA with the help of quasi floating bulk MOSFET and its performance comparison with reported results. Finally, Section 5 conclude the paper.

2 Gate-Driven Quasi Floating Bulk (GD-QFB) MOSFET Approach

GD-QFB MOS is one of the low voltage design approaches that removes the threshold limit of the transistor and enables MOSFET to operate at low voltage [6]. It also increases the transconductance over gate driven (GD) MOSFET. The basic GD-QFB-based MOSFET is shown in Fig. 2.

GD-QFB MOS provides an increased value of input capacitance in comparison to gate and bulk leads to an improved value of the transconductance that reduces the degradation in frequency due to the parasitic effect [6].

3 Gate-Driven (GD) OTA Design

Gate-driven two-stage OTA showed in fig. 3, which is the basic building block of the G_m-C filter. The first stage is the differential amplifier input stage with M1, M2 transistors, and the second stage has formed with the M5 and M8 transistors. The current compensation approach has used that provides the high-gain bandwidth product (GBW) and better swing [12, 13]. GD OTA is simulated using 180 nm SCL technology with the help of the cadence virtuoso IC 616 tool.

Simulated results show the magnitude response and phase response of GD OTA in Figs. 4 and 5 that provides DC gain is approximately 57 dB. The value of unity-gain bandwidth (UGB) is 47.07 MHz, and the phase margin (PM) is 41°.

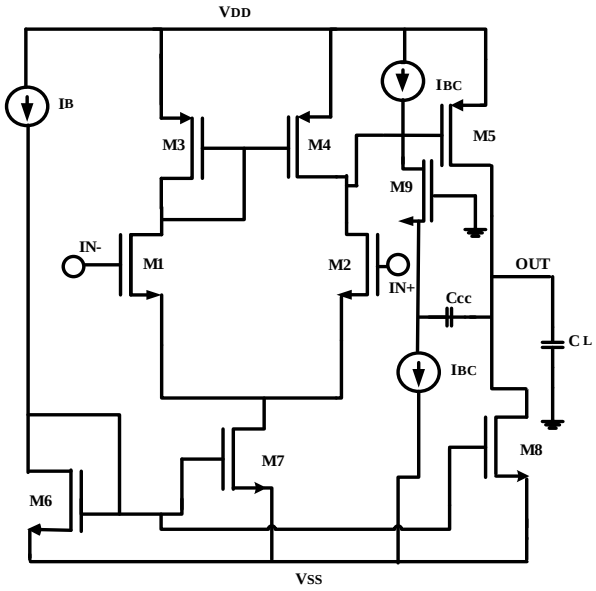

Fig. 3 GD OTA with current compensation [12, 13].

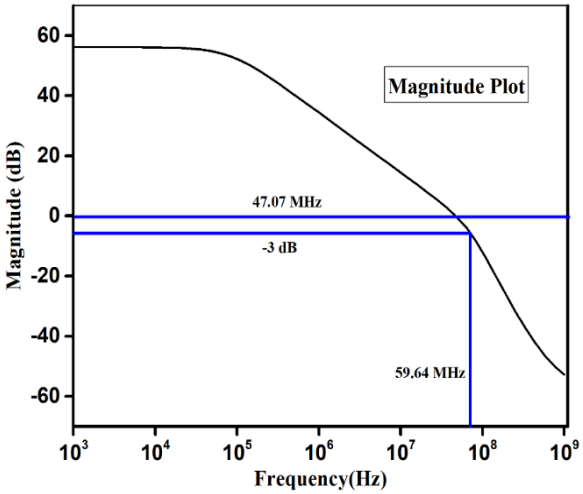

Fig. 4 GD OTA magnitude response.

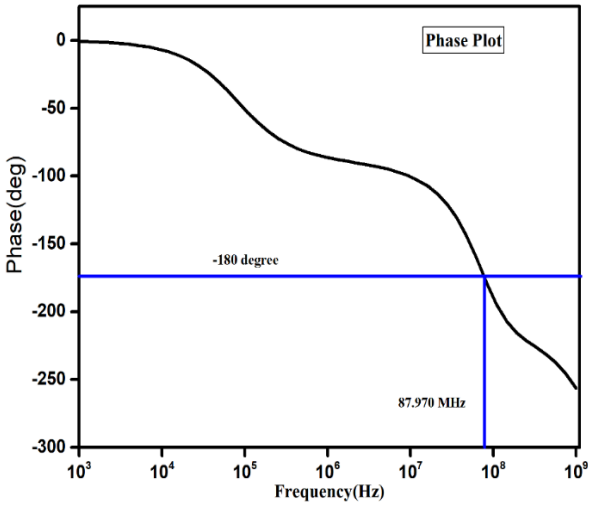

Fig. 5 GD OTA phase response.

4 Proposed Current Buffer Compensated GD-QFB MOS OTA

The proposed GD-QFB MOS-based two-stage OTA is depicted in fig. 6. Here, transistor M1 and M2 are GD-QFB MOSFETs that allows the circuit to operate at low input voltage. The current buffer approach preserves the output swing of OTA [12-13].

The first stage is a differential amplifier where IN+ and IN- is differential input supplied at the input of the transistor M1 and M2. Transistors M5 and M8 contribute to form the second stage of the proposed OTA. Current buffer compensation has been designed with the help of M9 transistor and current source I_{BC}. Cc and C_L represent the coupling capacitor and load capacitance as shown in Fig. 6. Table 1 shows the transistor sizing of current buffer compensated GD-QFB OTA that allows operating transistors in the saturation region. The size of the transistors M1 and M2 is adjusted to achieve the desirable transconductance of the OTA. Transistor M5 W/L is adjusted as per the PM requirement.

The small-signal analysis of the proposed GD- QFB MOS-based current OTA is depicted in Fig. 7. The small-signal model of proposed OTA shows that the transconductance of the GD-QFB MOSFET M1 and M2 has increased by factor k times of g_{mb} (bulk transconductance of the MOSFET).

The comparison between small-signal analysis of basic GD OTA and GD-QFB MOS-based OTA is shown in Table 2. GD-QFB MOS-based OTA shows the improvement in transconductance by kg_{mb}, where g_{mb} is bulk transconductance. k is the capacitor ratio of input capacitor/total capacitance that is less than unity. The DC gain of the GD-QFB OTA is increased by factor kg_{mb}. UGB of GD-QFB OTA also shows the improvement by kg_{mb} factor in comparison to GD OTA.

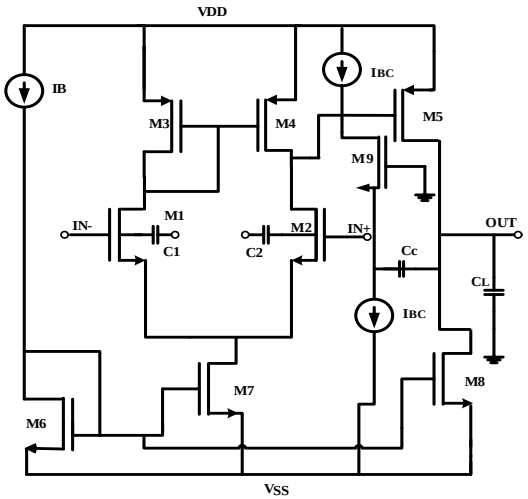

Fig. 6 Proposed current buffer compensated GD-QFB OTA.

Table 1 MOSFET aspect ratio.

Transistor	W/L [μm/μm]
M1, M2	8/1.2
M3, M4	17/1.2
M5, M6	22.5/1.2, 7/1.2
M7, M8	14/1.2, 10/1.2
M9	15/1.2

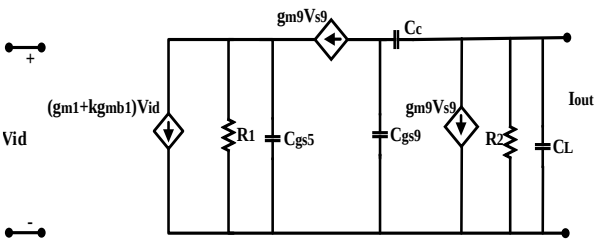

Fig. 7 Small-signal equivalent circuit of the proposed GD-QFB.

4.1 Proposed GD-QFB OTA Simulation Results and Discussion

The proposed GD-QFB OTA is depicted in Fig. 6 that is simulated using 180 nm SCL technology with the help of the cadence virtuoso IC 616 tool. Figs. 8 and 9 show the magnitude and phase response of the GD-QFB MOS-based OTA. GD-QFB MOS provides DC

Table 2 Mathematical analysis comparison of GD OTA and GD-QFB OTA.

Parameter	GD OTA	GD -QFB OTA
Transconductance	g_m	$g_m + kg_{mb}$
Output conductance	λI_d	$kg_{mb} + \lambda I_{dsat}$
DC gain	$A_o = g_{m1}g_{m5}R_1R_2$ ($R_1 = ro_2/ro_4$ $R_2 = ro_5/ro_8$)	$A_o = (g_{m1} + kg_{mb})\, g_{m5}R_1R_2$
UGB	$W_n = g_{m1}/C_c$	$W_n = g_{m1} + kg_{mb}/C_c$
Dominant pole frequency (W_p)	$W_p = 1/G_mR_1R_2C_c$	$W_p = 1/G_mR_1R_2C_c$

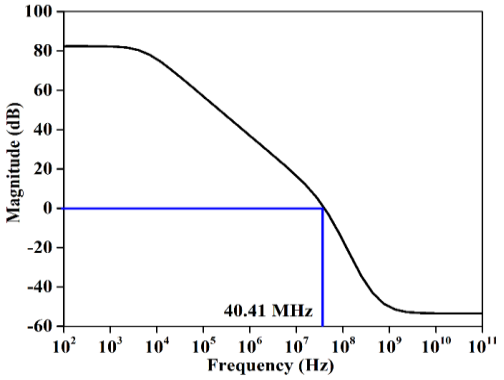

Fig. 8 GD-QFB MOS-based OTA magnitude response.

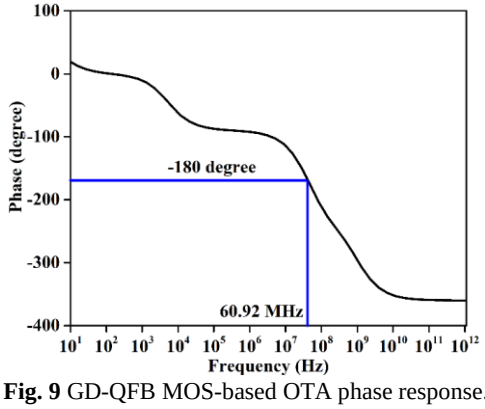

Fig. 9 GD-QFB MOS-based OTA phase response.

gain and unity gain frequency (UGB) of 82.41 dB and 49.41 MHz respectively. Table 3 shows the Monte-Carlo simulation results of GD-QFB OTA for 1000 iterations. The performance comparison as in table 3 shows that GD-QFB OTA provides a higher value of DC gain and CMRR of approximately 82.64 dB and 92.40 than GD OTA. But the phase margin of the proposed GD QFB OTA is reduced to 15.24°. The power consumption of GD-QFB MOS-based OTA is 187.32 µW at the supply voltage of 1V that is reduced by 34.79% in comparison to GD OTA. The proposed GD-QFB OTA showed the improvement in FOM. The improved value of FOM_S and FOM_L of the proposed OTA is 848.75 MHz.pF/mW and 211.93 V.pF/µsec.mW for small signal and large signal operations.

Table 3 also shows the comparison of the performance of the proposed GD-QFB OTA with reported results from the literature survey. The proposed GD-QFB OTA provides higher dc gain, CMRR, unity-gain bandwidth (UGB) along with a significant amount of reduction in power consumption in comparison to the reported results in the literature. Corner analysis has performed for proposed GD-QFB OTA to show the circuit robustness against process (TT, FF, SF, FS, and SS) and temperature variations (27ºC, +40ºC, and -40ºC) in Table 4.

4 GD-QFB MOS-based Gm-C Filter Design and Simulation Results

The loop filter is one of the essential building blocks of the PLL. Loop filter bandwidth plays an important in determining the PLL loop stability [10, 18]. Low loop filter bandwidth requires to reduce the noise in PLL, but high bandwidth is demanding to speed up the locking process [18]. Many loop filter design approaches are available in the literature [19-22]. Nowadays, reconfigurable low power PLL has a high demand in the market. So, G_m-C type loop filter is a better approach for reconfigurable PLL because it provides an automatic tuning facility. The architecture of the proposed GD-QFB MOS-based first-order G_m-C filter is shown in Fig. 10, where G_m represents the transconductance of OTA that can be adjusted as per filter requirement and C represents the capacitance required for G_m-C filter.

The transfer function of the proposed GD-QFB MOS-based first-order G_m-C filter is given as

$$\frac{V_{out}}{V_{in}} = \frac{G_m}{G_m + jw\,C} \tag{2}$$

$$\text{or } \frac{V_{out}}{V_{in}} = \frac{1}{1+\frac{jw}{G_m}} \tag{3}$$

$$\text{or } \frac{V_{out}}{V_{in}} = \frac{1}{1+\frac{jw}{w_o}} \tag{4}$$

where $w_o = G_m/C$ represents cut off frequency.

Table 3 Performance parameter of GD-QFB MOS-based OTA.

Parameter	GD OTA	GD-QFB OTA	[14]	[15]	[16]	[17]
Technology [nm]	180	180	500	180	180	500
Supply voltage [V]	1.8	1	±1.25	1.8	0.7	±1
DC gain [dB]	57	82.64	63.4	72	57.5	69
CMRR	63	92.40	83	--	19	91
UGB [MHz]	47.07	41.38	4.9	86.5	3	0.31
PM [degree]	41	15.24	83	50	60	89
Power consumption [µW]	287.3	187.32	437.5	11900	25.9	80
Load capacitance [pF]	4	4	25	200	20	70
FOM_S [MHz.pF/mW]	655.56	848.75	70	261.7	2361	75
FUM_L [V.pF/µsec.mW]	139.22	211.93	6.4	2.24	2204	0.56

Table 4 Performance parameter of proposed GD- QFB MOS-based OTA over process corner and temperature variations.

	Corner	DC gain [dB]	UGB [MHz]	PM [°]	GM [dB]	Power [µW]
Temperature	TT	82.41	40.41	15	5.05	188.72
T = +27º C	FF	82.86	43.78	17.83	5.16	189.84
	SS	82.87	40.78	14.24	4.83	188.53
	SF	83.08	41.65	17.08	5.35	189.98
	FS	82.19	4087	14.72	4.49	187.96
Temperature	TT	83.63	42.36	18.6	6.56	190.12
T = +40º C	FF	83.18	41.78	17.23	6.16	189.62
	SS	82.09	42.76	18.91	5.63	189.67
	SF	82.27	42.55	18.42	7.15	189.44
	FS	83.57	41.21	18.76	7.86	190.96
Temperature	TT	80.23	40.41	16.00	4.06	187.21
T = –40º C	FF	80.86	43.78	16.09	4.34	186.84
	SS	81.33	40.78	17.23	4.82	187.33
	SF	8154	41.90	16.70	5.12	186.90
	FS	81.93	42.79	16.01	4.73	185.66

The proposed first-order G_m-C filter is simulated with the help of a 180 nm CMOS process using cadence virtuoso IC 616 tool. Magnitude response of first-order G_m-C low pass filter is shown in Fig. 11 that shows GD-QFB MOS OTA-based G_m-C filter provides a cutoff frequency of 59.08 MHz. Phase response of the first order G_m-C filter is shown in Fig. 12.

Fig. 13 shows the magnitude plot of the G_m-C filter at different process corners to verify simulation at different process corners. The performance parameter of the G_m-C filter is summarized in Table 5. The proposed

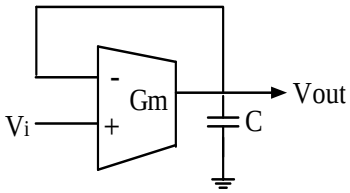

Fig. 10 GD–QFB MOS-based G_m-C first-order filter.

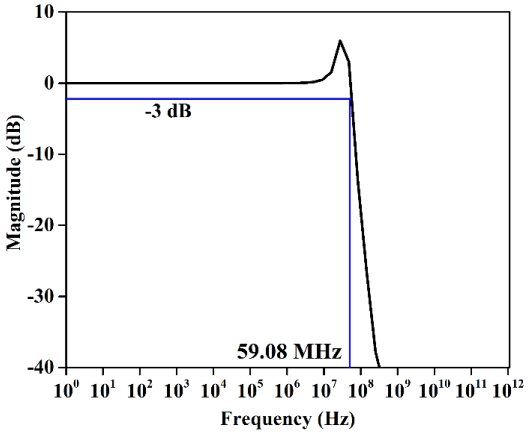

Fig. 11 GD–QFB MOS-based G_m-C first-order filter magnitude response.

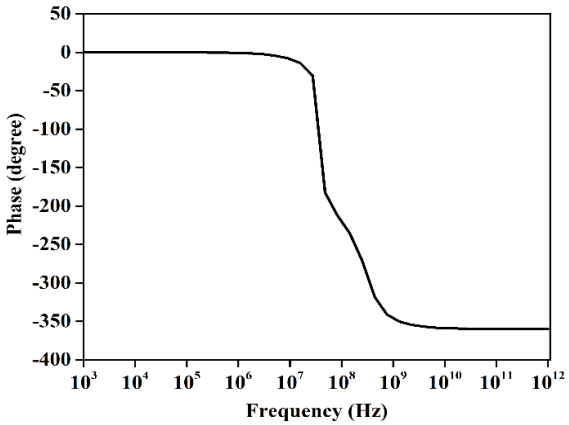

Fig. 12 GD–QFB MOS-based G_m-C first-order filter phase response.

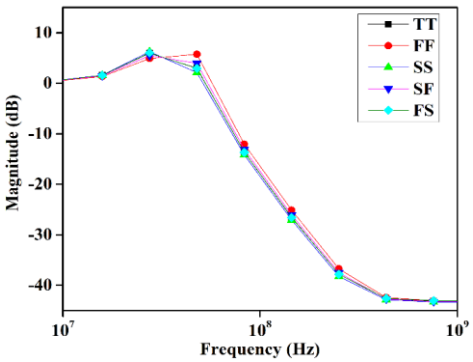

Fig. 13 G_m–C filter magnitude response at different processes.

Table 5 Performance parameter of GD-QFB MOS-based G_m-C Filter.

Parameter	GD-QFB OTA-based G_m–C filter	[18]	[19]	[20]	[21]
Technology [nm]	180	65	90	180	180
Supply voltage [V]	1	1	1	0.9	–
Cut off frequency [MHz]	59.08	73.6	1000	8	44
Filter type	G_m-C	Op-amp	G_m-C	G_m-C	G_m-C
Power consumption [µW]	188.31	360	2500	500	8500

Table 6 Performance parameter of GD-QFB OTA-based G_m-C filter over process corner and temperature variations.

	Corner	Cut off frequency [MHz]	Power consumption [µW]
Temperature	TT	59.08	188.31
T = +27° C	FF	61.55	189.57
	SS	56.21	188.19
	SF	59.29	187.54
	FS	59.17	188.19
Temperature	TT	57.21	187.23
T = +40° C	FF	58.05	188.49
	SS	55.23	186.16
	SF	56.43	187.33
	FS	55.87	186.66
Temperature	TT	57.60	187.21
T = -40° C	FF	58.87	186.36
	SS	54.11	185.62
	SF	57.26	187.75
	FS	57.26	184.09

G_m-C filter operates at a cut off frequency of 59.08 MHz and consumes the power consumption of 188.31 µW at the supply voltage of 1V. Further, the proposed G_m-C filter has compared with the reported results in the literature. The proposed G_m-C filter consumes less amount of power consumption for the same supply voltage requirement of 1V in reported results.

The robustness of G_m-C filter is analyzed with the help of process corner and temperature variations analysis as depicted in table 6. Here, the circuit is simulated at temperature variation of respectively 27º C, +40º C, and –40º C for different process corners. The proposed circuit can be used for the designing of low power reconfigurable PLL.

5 Conclusion

In this paper, GD-QFB MOS differential input two-stage OTA has been presented. The proposed OTA utilizes the current compensated technique for proper adjustment of the dominant pole. The use of GD- QFB MOS at OTA input allows the circuit to operate the circuit at a low power requirement. The simulation results show the significant improvement in dc gain, CMRR, and reduction in the power consumption of OTA. However, the proposed OTA suffers from low PM limitations. Further, the proposed OTA is used in the design of the tunable G_m-C filter for low power PLL applications. The proposed GD- QFB MOS-based G_m-C filter can be further used in the designing of 1-3 GHz PLL.

Acknowledgment

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