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Single Source Cross-Connected Reduced Activated Switched-Capacitor Multilevel Inverter (S^2C^2RASCMLI) with Self-Voltage Balancing for Horizontal/Vertical Extension

O. G Murugan*(C.A.), J. Arumugam**, S. Velliangiri***

Abstract: Single Source Cross Connected Reduced Activated Switched-Capacitor Multilevel Inverter (S^2C^2RASCMLI) accompanied by fewer active switching components is appealing to nine-level of voltage with its simplicity and a solid network. In AC power distribution systems, multi-level inverters are used as DC-to-AC converter operations to achieve the desired output magnitude and frequency. It is employed for the smooth operation of electrical machines. The proposed S^2C^2RASCMIL cell yields a nine-level voltage with ten switches, nine driver signals, and two flying capacitors for dynamic load operation with reduced active switches. It has the capability of boosting the input voltage double the times. The proposed multilevel inverter operated on nine switching modes and in each mode, three switches have been conducted. It can be extended horizontal and/or vertical structure to produce more levels of output voltages. The hardware prototype was made and the results have been presented. To demonstrate the advantages of the new proposed multilevel inverter topology, a comprehensive comparison with a few other similar multilevel inverter configurations is done. Analysis and simulation output waveforms for a variety of load conditions were tested to check the feasibility of the proposed new multi-level inverter. The proposed MLI offers better performance than existing multilevel inverters.

Keywords: H-Bridge, Multi-Level Inverter, Switched Capacitor, Voltage Balancing.

1 Introduction

MULTI-LEVEL inverters (MLIs) are used in a wide range of applications, comprising industrial drives and renewable energy generation. Switches with high-quality output voltage and low voltage stresses are MLIs' key advantages [1]. The input sources, flying capacitor and H-Bridge are the most widely used multi-level inverter structures, because of their benefits: fewer capacitors, switches, input sources, automated capacitor voltage balance, and the ability to boost input voltage with maximum voltage gain [2]. These configurations have been extensively studied and are well-proven in industry sectors [3]. The boosting factor of the switched-capacitor inverters is critical in grids powered by renewable energy sources, as the voltage output given by renewable energy cells [4] has been so much lower than the necessary grid voltage's peak. Power converters serve as important in smart grids because of their benefits such as reliability, consistency, temperature control and high energy efficiency [5]. Multi-level inverters are a special variant of converter that has many structural

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advantages such as simple extension [6], minimal voltage stress (*dv*/*dt*), fair load contribution, and effective power extraction, making them ideal for a variety of high-power applications [7]. Switched-capacitor multilevel inverters are the most commonly utilized of the various MLIs due to their advantages in voltage boost over traditional MLIs with fewer DC sources [8]. Cascaded MLIs produce more levels of the voltage while reducing the number of devices used, but this results in increased voltage block plus it's not guaranteed for the function of voltage boost [9, 10].

The switched capacitor topology helps to reduce the number of voltage supplies. The packed E-cell topology is a capacitor-based topology that was proposed in [11, 12]. The output waveform can be generated at nine voltage levels using two voltage supply and two capacitors; however, the topology lacks input voltage boosting. Similar to [13] suggested nine-level inverter structures with two DC voltage supplies including two voltage regulating capacitors. Two new MLI configurations with two DC voltage supplies as well as two capacitors have been proposed by the researchers in [14]. Both topologies produce nine voltage levels around the load. To shift supply polarity, both MLI topologies use an H-bridge, which necessitates the use of higher-voltage switches. The topologies cannot often boost.

Mostly in the latest multilevel inverter topology, several sub-multilevel converter groups and complete bridge converters are used [15]. While [16] proposes a basic configuration, multiple divided DC voltage sources are always needed. [17] Invented the coupled-inductor method for multilevel inverters. Although the architectures are simplified, expanding this methodology to higher-level applications is difficult. Unique topologies focused on the switched capacitor [18] and boosting technologies were introduced in [19], however, their performance voltage levels are restricted to thirteen, seven, and nine comparatively. On the other hand, the multilevel topology used in [20] can be increased to higher levels. Utilizing the higher number of conduction switches tends to raise the price and element count in signal conditioning circuits. The switched capacitor technique inverter used in lots of applications often connects a DC-DC converter and H-bridge [21].

In the suggested topology, only a single DC voltage supply is connected. In Addition, several issues like voltage balancing, the higher number of conduction switches and more signal conditioning circuitry are avoided. The DC-DC transformation branch, which is made up of several Switched Cells (SC) is the most critical part of the entire topology. Two capacitors, four switches, and two diodes make up every SC except the last cell. As a result, by varying the number of switched-capacitor cells used, the output voltage levels of a proposed inverter can be varied.

2 Proposed Topology

2.1 The Configuration of the Suggested Topology

Figure 1 shows the proposed nine-level S^2C^2RASCMLI topology. To attain the desired voltage level, the H-bridge is inserted in the backyard to change the polarity and then two capacitors are connected in series.

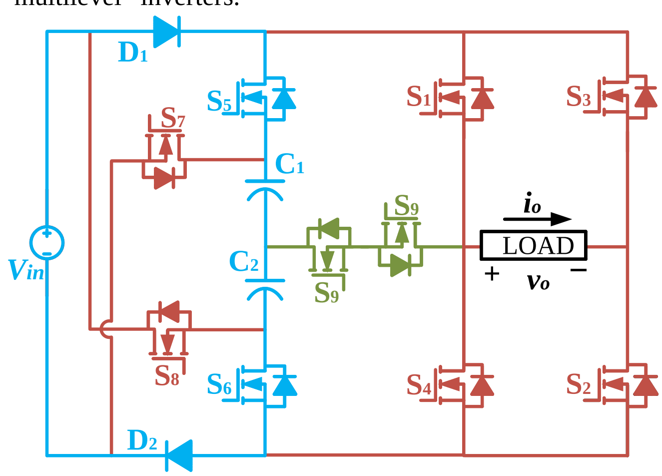

Fig. 1 Proposed nine-level inverter topology.

A single source of DC voltage V_{in}, two flying capacitors C_1 & C_2, two power diodes D_1 & D_2 and ten semiconductor switches S_1-S_9 (S_9 back-to-back connection) are also used in the proposed nine-level S^2C^2RASCMLI for producing a voltage at its peak that is double the input voltage and has nine different output voltage levels (0, $\pm V_{in}/2$, $\pm V_{in}$, $\pm 3V_{in}/2$, $\pm 2V_{in}$).

2.2 Operational Modes of the Proposed S[2]C[2]RASCMLI

Table 1 shows the switching patterns, states of diodes, and capacitors at each voltage level for the proposed nine-level inverter. And a better explanation, the various modes of action and current direction are also shown in Figure 2(a) – Figure 2(i) for both positive and negative half-cycle. Where i_o denotes the current's path. Both capacitors were charged during $\pm V_{in}/2$ and $\pm V_{in}$ level, resulting in an output voltage equal to $\pm V_{in}/2$ and $\pm V_{in}$. During $\pm 3V_{in}/2$, capacitor C_2 is discharged, resulting in an output voltage of $\pm 3V_{in}/2$. While both capacitors C_2 and C_1 are discharged collectively during $\pm 2V_{in}$, producing an output voltage equal to $\pm 2V_{in}$, and so on, both capacitors are charged and discharged collectively during $\pm V_{in}$ and $\pm 2V_{in}$ respectively.

Table 1 Switching patterns, states of diodes, and capacitors at each voltage level.

Voltage Levels	Switches in H-Bridge Circuit				Switches					Diodes		Capacitors	
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	D_1	D_2	C_1	C_2
$+2V_{in}$	1	1	0	0	1	0	0	1	0	R	F	DS	DS
$+3V_{in}/2$	0	1	0	0	0	0	0	1	1	R	F	NC	DS
$+V_{in}$	1	1	0	0	1	1	0	0	0	F	F	CH	CH
$+V_{in}/2$	0	1	0	0	1	1	0	0	1	F	F	CH	CH
0	0	1	0	1	1	1	0	0	0	F	F	CH	CH
$-V_{in}/2$	0	0	1	0	1	1	0	0	1	F	F	CH	CH
$-V_{in}$	0	0	1	1	1	1	0	0	0	F	F	CH	CH
$-3V_{in}/2$	0	0	1	0	0	0	1	0	1	F	R	DS	NC
$-2V_{in}$	0	0	1	1	0	1	1	0	0	F	R	DS	DS

In this case, 1 or 0 whether the switches are ON or OFF; F or R indicates whether the diodes are forward or reverse biased; and CH, DS, or NC indicates whether the capacitors are charged, discharged, or unchanged.

In this case, 1 or 0 whether the switches are ON or OFF; F or R indicates whether the diodes are forward or reverse biased; and CH, DS, or NC indicates whether the capacitors are charged, discharged, or unchanged.

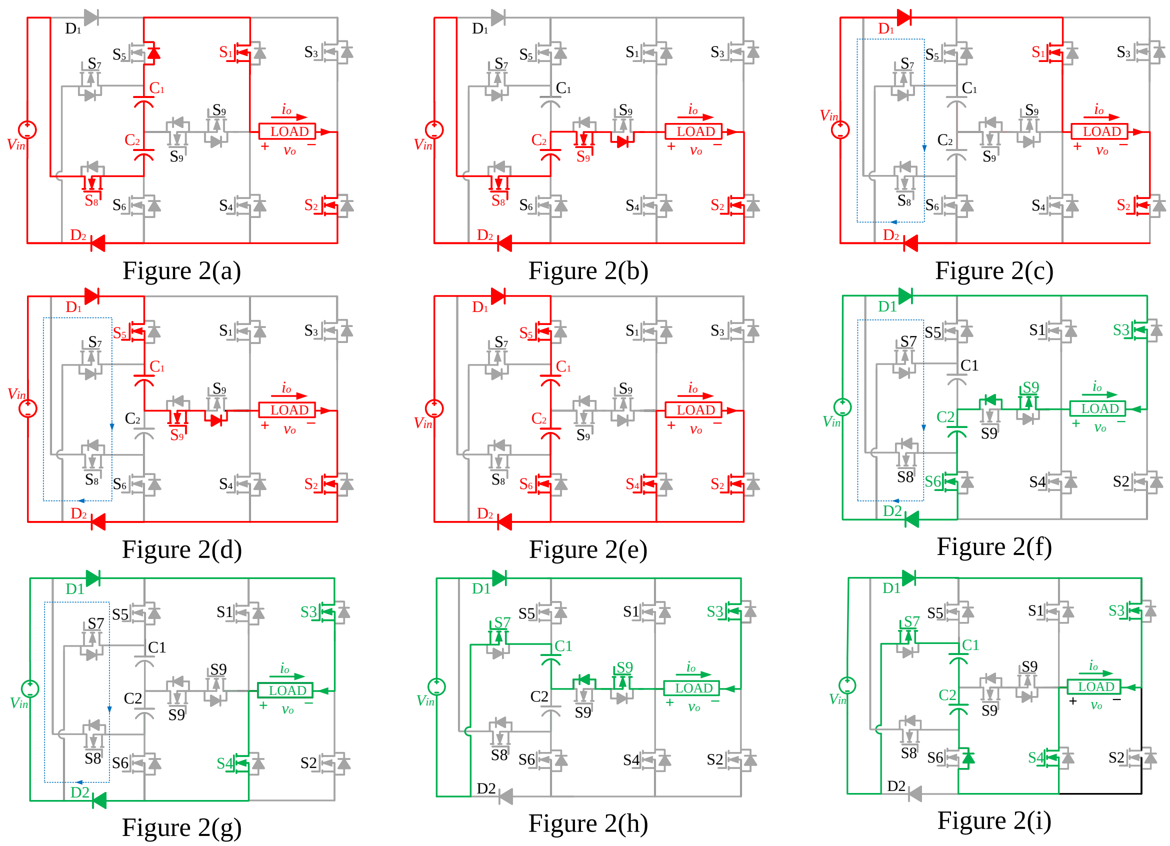

Figure 2(a) $V_o = +2V_{in}$, Figure 2(b) $V_o = +3V_{in}/2$, Figure 2(c) $V_o = +V_{in}$, Figure 2 (d) $V_o = +V_{in}/2$, Figure 2 (e) $V_o = 0$, Figure 2 (f) $V_o = -V_{in}/2$, Figure 2 (g) $V_o = -V_{in}$, Figure 2 (h) $V_o = -3V_{in}/2$, Figure 2 (i) $V_o = -2V_{in}$.

Fig. 2 Various modes of action and current direction.

The most important properties of the proposed nine-level S^2C^2RASCMLI are (i) produces an output voltage that is double the applied input voltage (ii) Only three active switches and a couple of capacitors and diodes help to achieve the required output voltage level on each mode (iii) With less difficulty, self-balancing and self-voltage boosting maintain by the circuit and it does not need external circuits to balance capacitor voltage. (iv) Reduced switches for extension switched cells.

3 Extension of the Proposed Nine-Level S^2C^2RASCMLI

To achieve the necessary performance, the proposed nine-level S^2C^2RASCMLI can be structurally extended to produce a greater number of voltage levels in all directions. There are two ways of extension such as the horizontal and vertical extension. The horizontal and vertical extension of the proposed nine-level S^2C^2RASCMLI is shown in Figure 3(a) and Figure 3(b) respectively to produce higher voltage levels. The cell is expended as first cell, second cell...N^{th} cell.

3.1 Horizontal Extension

Every cell contains the same unit of structure up to the N^{th} cell except H–bridge interconnected switch S_9. The 1^{st} cell switches are S_{51}, S_{61}, S_{71}, & S_{81}; while diodes D_{11} & D_{21} and capacitors C_{11} & C_{21}. Similarly, 2^{nd} Cell switches are S_{52}, S_{62}, S_{72}, & S_{82}; while diodes D_{12} & D_{22} and capacitors C_{12} & C_{22} are expended in the same manner up to N^{th} cell. Here the capacitors are linked parallel to boost the voltage levels of an inverter. Further, the working of the proposed nine-level S^2C^2RASCMLI (HE) is discussed with the switching Table 2.

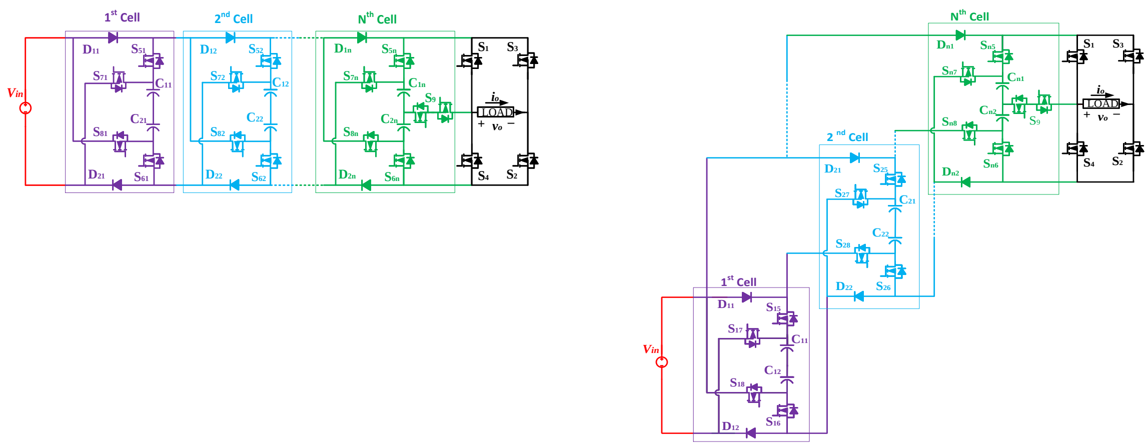

Figure 3(a) Figure 3(b)

Figure 3(a) Horizontal Extension, Figure 3(b) Vertical Extension.

Fig. 3 Extension of proposed nine-level S²C²RASCMLI.

Table 2 depicts the proposed nine-level S²C²RASCMLI (HE) switching sequence, which is depicted in Figure 3(a). Also, states of the capacitor such as charging, discharging and "NO" change details are mentioned in Table 2. For the low-level voltage output, the capacitors are charging long period. If chooses a high voltage level, the capacitor is discharging from higher to lower order number as shown in Table 2.

Further, the generalized equation (1) – equation (7) is given to construct the proposed nine-level S²C²RASCMLI (HE).

$$N_{IS} = 4n + 2\ (Included\ S_9) \tag{1}$$

$$N_{DC} = 4n + 1\ (Included\ S_9) \tag{2}$$

$$N_{VL} = 4(n+1) \tag{3}$$

$$N_C = 2(n-1) \tag{4}$$

$$N_D = 2(n-1) \tag{5}$$

$$V_{MOV} = nV_{in} \tag{6}$$

$$V_{in}: V_o = 1: n \tag{7}$$

where N_{IS} represents the number of power electronics switches, N_{DC} represents the number of driver circuits, N_{VL} represents the number of voltage level, N_C represents the number of flying capacitors, N_D represents the number of power Diodes, V_{MOV} represents Maximum Output Voltage And n represents the maximum voltage gain generated by the N^{th} cell with a single source, as an inverter satisfied the condition $n \geq 2$.

3.2 Vertical Extension

Figure 3(b) depicts the proposed nine-level S²C²RASCMLI I's the vertical extension (VE). It is expended as First cell, second cell...N^{th} cell. Every cell contains the same unit of structure up to the N^{th} cell which has H–bridge interconnected solid switch S_9. The 1^{st} cell switches are S_{15}, S_{16}, S_{17}, & S_{18}; while diodes D_{11} & D_{12} and capacitors C_{11} & C_{12}. Similarly, 2nd Cell switches are S_{25}, S_{26}, S_{27}, & S_{28}; while diodes D_{21} & D_{22} and capacitors C_{21} & C_{22} are expended in the same manner up to Nth cell. Here all the capacitors are connected parallel to boost the voltage levels of an inverter. Figure 3(b) shows how equation (8) – equation (14) leads to nine-level S²C²RASCMLI (VE) for expanding up to n.

$$N_{IS} = 4n + 2\ (Included\ S_9) \tag{8}$$

$$N_{DC} = 4n + 1\ (Included\ S_9) \tag{9}$$

$$N_{VL} = 4(n+1) \tag{10}$$

$$N_C = 2(n-1) \tag{11}$$

$$N_D = 2(n-1) \tag{12}$$

$$V_{MOV} = nV_{in} \tag{13}$$

$$V_{in}: V_o = 1: n \tag{14}$$

where n denotes the maximum voltage gain produced by the Nth cell with a single source, and $n \geq 2$ denotes that the inverter fulfilled the condition. Table 3 shows the generalized switching pattern of the nine-level S²C²RASCMLI (VE) for $(n+1)$ V_{in} voltage levels generation. States of the capacitor such as charging, discharging and no change details are mentioned in Table 3.

Table 2 The switching pattern of the proposed nine-level S^2C^2RASCMLI (HE).

Voltage Levels	Switches in H-Bridge Circuit	"ON" state Switches					Conducting Diodes		States of Capacitors	
	S_1,S_2,S_3,S	$S_{51},S_{52},\ldots S_{5n}$	$S_{61},S_{62},\ldots S_{6n}$	$S_{71},S_{72},\ldots S_{7n}$	$S_{81},S_{82},\ldots S_{8n}$	S_9	$D_{11},D_{12},\ldots D_{1n}$	$D_{21},D_{22},\ldots D_{2n}$	$C_{11},C_{12},\ldots C_{1n}$	$C_{21},C_{22},\ldots C_{2n}$
$+(n+1)V_{in}$	S_1,S_2	---	---	---	$S_{81},S_{82},\ldots S_{8n}$	---	---	$D_{21},D_{22},\ldots D_{2n}$	$C_{11d},C_{12d},\ldots C_{1nd}$	$C_{21d},C_{22d},\ldots C_{2nd}$
…	…	…	…	…	…	…	…	…	…	…
$+5V_{in}/2$	S_2	$S_{51},\ldots S_{5(n-2)}$	$S_{61},\ldots S_{6(n-2)}$	---	$S_{8(n-1)},S_{8n}$	S_9	$D_{11},\ldots D_{1(n-2)}$	$D_{21},D_{22},\ldots D_{2n}$	$C_{11},C_{12},\ldots C_{1(n-1)d},C_{1n-}$	$C_{21},C_{22},\ldots C_{2(n-1)d},C_{2nd}$
$+3V_{in}/2$	S_2	$S_{51},\ldots S_{5(n-1)}$	$S_{61},\ldots S_{6(n-1)}$	---	S_{8n}	S_9	$D_{11},\ldots D_{1(n-1)}$	$D_{21},D_{22},\ldots D_{2n}$	$C_{11},C_{12},\ldots C_{1n-}$	$C_{21},C_{22},\ldots C_{2nd}$
$+V_{in}/2$	S_2	$S_{51},S_{52},\ldots S_{5n}$	$S_{61},S_{62},\ldots S_{6n}$	---	---	S_9	$D_{11},D_{12},\ldots D_{1n}$	$D_{21},D_{22},\ldots D_{2n}$	$C_{11},C_{12},\ldots C_{1n}$	$C_{21},C_{22},\ldots C_{2n}$
0	S_2,S_4	$S_{51},S_{52},\ldots S_{5n}$	$S_{61},S_{62},\ldots S_{6n}$	---	---	---	$D_{11},D_{12},\ldots D_{1n}$	$D_{21},D_{22},\ldots D_{2n}$	$C_{11},C_{12},\ldots C_{1n}$	$C_{21},C_{22},\ldots C_{2n}$
$-V_{in}/2$	S_3	$S_{51},S_{52},\ldots S_5$	$S_{61},S_{62},\ldots S_{6n}$	----	----	S_9	$D_{11},D_{12},\ldots D_{1n}$	$D_{21},D_{22},\ldots D_{2n}$	$C_{11},C_{12},\ldots C_{1n}$	$C_{21},C_{22},\ldots C_{2n}$
…	…	…	…	…	…	…	…	…	…	…
$-(n+1)V_{in}$	S_3,S_4	---	---	$S_{71},S_{72},\ldots S_{7n}$	----	--	$D_{12},D_{12},\ldots D_{1n}$	---	$C_{11d},C_{12d},\ldots C_{1nd}$	$C_{21d},C_{22d},\ldots C_{2nd}$

---: "OFF" state; C_{1x} & C_{2x}: state of charging; C_{1xd} & C_{2xd}: state of discharging; C_{1x-} & C_{2x-}: state of "NO" Change where x = 1, 2 ...n.

Table 3 The switching pattern of the proposed nine-level S^{2}C^{2}RASCMLI (VE).

Voltage Levels	Switches in H-Bridge Circuit	"ON" state Switches					Conducting Diodes		States of Capacitors	
	S_1,S_2,S_3,S_4	$S_{15},S_{25},\ldots S_{n5}$	$S_{61},S_{26},\ldots S_{n6}$	$S_{17},S_{27},\ldots S_{n7}$	$S_{18},S_{28},\ldots S_{n8}$	S_9	$D_{11},D_{21},\ldots D_{n1}$	$D_{12},D_{22},\ldots D_{n2}$	$C_{11},C_{21},\ldots C_{n1}$	$C_{212},C_{22},\ldots C_{2n2}$
$+(n+1)V_{in}$	S_1,S_2	---	---	---	$S_{18}, S_{28},\ldots S_{n8}$	---	---	$D_{12},D_{22},\ldots D_{n2}$	$C_{11d},C_{21d},\ldots C_{n1d}$	$C_{12d},C_{22d},\ldots C_{n2d}$
…	…	…	…	…	…	…	…	…	…	…
$+V_{in}/2$	S_2	$S_{15},S_{25},\ldots S_{n5}$	$S_{16},S_{26},\ldots S_{n6}$	---	---	S_9	$D_{11},D_{21},\ldots D_{n1}$	$D_{12},D_{22},\ldots D_{n2}$	$C_{11},C_{21},\ldots C_{n1}$	$C_{12},C_{22},\ldots C_{n2}$
0	S_2,S_4	$S_{15},S_{25},\ldots S_{n5}$	$S_{16},S_{26},\ldots S_{n6}$	---	---	---	$D_{11},D_{21},\ldots D_{n1}$	$D_{12},D_{22},\ldots D_{n2}$	$C_{11},C_{21},\ldots C_{n1}$	$C_{12},C_{22},\ldots C_{n2}$
$-V_{in}/2$	S_3	$S_{15},S_{25},\ldots S_{n5}$	$S_{16},S_{26},\ldots S_{n6}$	----	----	S_9	$D_{11},D_{21},\ldots D_{n1}$	$D_{12},D_{22},\ldots D_{n2}$	$C_{11},C_{21},\ldots C_{n1}$	$C_{12},C_{22},\ldots C_{n2}$
$-3V_{in}/2$	S_3	$S_{15},\ldots S_{(n-2)5}$	$S_{16},\ldots S_{(n-2)6}$	S_{n7}	---	S_9	$D_{11},D_{21},\ldots D_{n1}$	$D_{12},\ldots D_{(n-1)2}$	$C_{11},C_{21},\ldots C_{n1d}$	$C_{12},C_{22},\ldots C_{n2-}$
$-5V_{in}/2$	S_3	$S_{15},\ldots S_{(n-2)5}$	$S_{16},\ldots S_{(n-2)6}$	$S_{(n-1)7}, S_{n7}$	---	S_9	$D_{11},D_{21},\ldots D_{n1}$	$D_{12},\ldots D_{(n-2)2}$	$C_{11},C_{21},\ldots C_{(n-1)1d},C_{n1d}$	$C_{12},C_{22},\ldots C_{(n-12)d},C_{n2-}$
…	…	…	…	…	…	…	…	…	…	…
$-(n+1)V_{in}$	S_3,S_4	---	---	$S_{17}, S_{27},\ldots S_{n7}$	----	---	$D_{11},D_{21},\ldots D_{n1}$	---	$C_{11d},C_{21d},\ldots C_{n1d}$	$C_{12d},C_{2d},\ldots C_{n2d}$

---: "OFF" state; C_{x1} & C_{x2}: state of charging; C_{x1d} & C_{x2d}: state of discharging; C_{x1-} & C_{x2-}: state of "NO" Change where x = 1, 2 ...n.

4 Modulation Technique

The desired sinusoid output voltage in typical multilevel inverters produced by the staircase waveform [10, 12]. To get better approximate sinusoidal waveforms by increasing the number of levels, but it is increasing the number of component cost and complexity of the signal circuit. However, designer always stays with the quality of output, cost and efficiency of the inverters. The proposed and extended cell of the inverter constantly stays with a reduced component with reduced conduction switches to minimize the complexity of signal conditioning circuits.

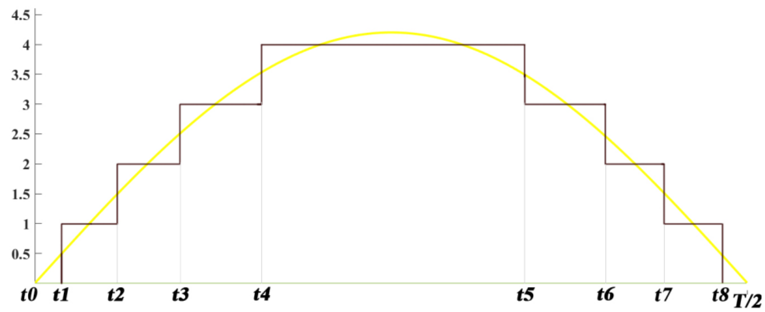

Fig 4 Modulation strategy for the half-cycle fundamental frequency.

The modulation strategy for half-cycle fundamental frequency (f) helps to calculate the highest voltage level of the inverter from the given sinusoidal signal as shown in Figure 4. An electric grid of the nation synthesizes the frequency and output voltage. This application takes the frequency f = 50Hz. As per the operation of the circuit, the transition time of each voltage level is calculated by the given equation (15).

$$Ts = \frac{1}{\omega} arcsin\left(\frac{2s-1}{N-1}\right) \quad where\ s = 1,2,\dots,8;\ \ \omega = 2\pi f \tag{15}$$

t_1 = 4.000 ×10^{-4}ms; t_2 = 1.223 ×10^{-3}ms;
t_3 = 2.156 ×10^{-3}ms; t_4 = 3.399 ×10^{-3}ms;
t_5 = 6.666 ×10^{-3}ms; t_6 = 7.854 ×10^{-3}ms;
t_7 = 8.788 ×10^{-3}ms; t_8 = 9.663 ×10^{-3}ms;
t_9 = T/2 = 0.0 1ms;

The nine levels of the proposed inverter staircase are 0, V_{in}/2, V_{in}, 3V_{in}/2, 2V_{in} getting from the transition time of t_1 - t_9 (For negative half-cycle similar strategy is used).

5 Design of Voltage Balancing Capacitors

The capacitors have two discharging cycles for every half-cycle, according to the switching sequence mentioned in Table 1.

$$C_1\text{: } \theta_4 \text{ - } \theta_5\text{; } \theta_5 \text{ - } \theta_6$$
$$C_2\text{: } \theta_3 \text{ - } \theta_4\text{; } \theta_4 \text{ - } \theta_5$$

The capacitor voltage ripples ΔV_{C_1} and ΔV_{C_2} are calculated from equation (16) and equation (17).

$$\Delta V_{C_1} = \frac{1}{2\pi f C_1}\int_{\theta_4}^{\pi-\theta_3} i_{C_1} d\theta = \frac{1}{2\pi f C_1}\int_{\theta_4}^{\pi-\theta_3} i_o d\theta \tag{16}$$

$$\Delta V_{C_2} = \frac{1}{2\pi f C_2}\int_{\theta_3}^{\pi-\theta_5} i_{C_2} d\theta = \frac{1}{2\pi f C_2}\int_{\theta_3}^{\pi-\theta_5} i_o d\theta \tag{17}$$

where f is the fundamental frequency for switching; i_o is the output current, resulting in $\Delta V_{C_1} = \Delta V_{C_2} =$ 887mV. It can be noted that two capacitors voltage ripples are equal because of its same interval. From equation (16) and equation (17), the output current is the same in discharging circuit mode operation of output voltage levels 3V_{in}/2 and 2V_{in}. A benefit of the proposed inverter is that it produces equivalent capacitor values by implementing a ripple voltage of 7.5% of the capacitor's maximum voltage. As a result, it has been selected $C_1 = C_2 = 4700\ \mu F$.

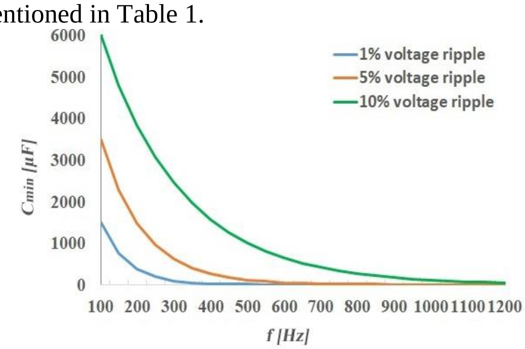

Figure 5(a)

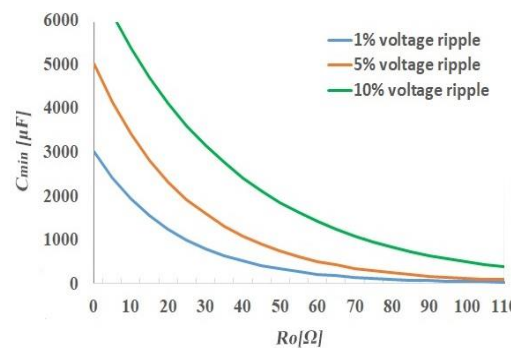

Figure 5 (b)

Fig. 5 Curves of minimal capacitance vs. output frequency and resistive load.

In addition, Figure 5 shows Curves of minimal capacitance vs. output frequency and resistive load (Ro). It has been discovered as the rated power dissipation increases, the capacitance must be increased to maintain the ripple voltage in an acceptable range Figure 5(b), and that the greater the frequency the smaller the capacitance Figure 5(a).

6 Analysis of Power Losses

The conduction and switching losses are measured using the reference [22] equations and procedure. The forward voltage drops of the diodes D_1 & D_2 are represented in Table 4 by V_{F_1} and V_{F_2} respectively.

Table 4 Specifications of components.

Component	Resistance value
Capacitor C_1 & C_2	4700 µF, r_c = 0.124 Ω
Conduction resistance of switches S_1- S_6	r_h & r_f = 0.032 Ω
Conduction resistance of switches S_7 & S_8	r_s = 0.0092 Ω
Conduction resistance of switches S_9	r_l = 0.0422 Ω
Diode D_1 & D_2	V_{F_1} & V_{F_2} = 0.964 V

where r_l is the conduction resistance of the switch S_9, r_h is the conduction resistance of H-bridge resistance S_1 - S_4. R_o is the load resistance of the inverter. r_c is the series resistance (equivalent) of a capacitor, r_f is the conduction resistance of the S_5 & S_6, r_s is the conduction resistance of the S_7 & S_8. The power losses are calculated using the values given in Table 4.

(i) When the capacitor charges at output voltage levels of 0, $V_{in}/2$ and V_{in} from the parallel-connected voltage source, the capacitor losses happen with each half-cycle. The respected capacitor power losses can be expresses as equation (18).

$$P_{(loss_{capacitor})} = 3f\sum_{j=1}^{2} \Delta V_{C_j} \tag{18}$$

where $\Delta V_{C_j} = C_j\ (\Delta V_{C_j}\ (V_{F_1} + V_{F_2}) + \Delta V^2 C_j\ );\ j = 1,\ 2.$

$$P_{(loss\_capacitor\ )} =$$

$$3fC_1\ (\Delta V_{C_1}\ (V_{F_1} + V_{F_2}) + \Delta V^2 C_1) + 3fC_2\ (\Delta V_{C_2}\ (V_{F_1} + V_{F_2}) + \Delta V^2 C_2)$$

(ii) The load receives the energy from the input source at $V_{in}/2$ and V_{in} levels. During the period, the conduction loss of capacitor is the calculation from the equation (19) and equation (20).

$$P_{(loss-disch1)} = 4f\ \frac{\theta_2 - \theta_1}{2\pi f}\left[(r_l + r_h)\left(\frac{\frac{V_{in}}{2} - (V_{F_1} + V_{F_2})}{R_o + r_l + r_h}\right)^2 + (V_{F_1} + V_{F_2})\left(\frac{\frac{V_{in}}{2} - (V_{F_1} + V_{F_2})}{R_o + r_l + r_h}\right)\right] \tag{19}$$

$$P_{(loss\_disch2)} = 4f\ \frac{\theta_3 - \theta_2}{2\pi f}\left[2r_h\ \left(\frac{V_{in} - (V_{F_1} + V_{F_2})}{R_o + 2r_h}\right)^2 + (V_{F_1} + V_{F_2})\left(\frac{V_{in} - (V_{F_1} + V_{F_2})}{R_o + 2r_h}\right)\right] \tag{20}$$

(iii) The discharging phase of the capacitor losses calculated in the levels of $3V_{in}/2$ and $2V_{in}$ by equation (21).
Where I_1 & I_2 : The current in the discharging phase of the capacitors.

$$P_{(loss\_disch3\ )} = (3\Delta V_{C_{d1}} + 3\Delta V_{C_{d2}}) \tag{21}$$

where:

$$\Delta V_{C_{d1}} += I_1^2 r_1\ \frac{\theta_4 - \theta_3}{2\pi f} = \left(\frac{\frac{3}{2}V_{in}}{R_o + r_1}\right)^2\ r_1\ \frac{\theta_4 - \theta_3}{2\pi f}$$

$$r_1 = r_c + r_f + r_s + r_l + r_h$$

$$\Delta V_{C_{d2}} = I_2^2 r_2\ \frac{\pi - 2\theta_4}{2\pi f} = \left(\frac{4V_{in}}{R_o + r_2}\right)^2\ r_2\ \frac{\pi - 2\theta_4}{2\pi f}$$

$$r_2 = 2 \times r_c + r_f + r_s + 2 \times r_h$$

(iv) Switching losses (equation (22)) associated with each switch's ON and OFF of P_{Switch}, where ($N_{(Switch)}$) is the number of switches in the topology.

$$P_{(Switch\_total)} = \sum_{q=1}^{N(Switch)}\left[\sum_{p=1}^{N(p)} P_{Switch,on(pq)} + \sum_{p=1}^{N(p)} P_{Switch,off(pq)}\right] \tag{22}$$

The switching power losses on the q^{th} turn-ON the p in a loop is represented by $P_{Switch,on(pq)}$ turn-OFF the switch in the same way with the same switch on conduction failure. In a switching loop, $N_{(p)}$ donates the turn-ON/turn-OFF switch p. In other words, q=1, 2, ..., $N_{(p)}$. $V_{off_{state(pq)}}$ is the OFF-state voltage p after an OFF-action q and $I_{on_{state1,(pq)}}$ the current throughout switch p before an ON of q, the expression in the equation (22) is calculated with equation (23) and equation (24).

$$P_{(Switch,on(pq)} = \frac{f V_{off_{state(pq)}} I_{on_{state1,(pq)}} t_{on}}{6} \tag{23}$$

$$P_{(Switch,off(pq))} = \frac{f V_{off_{state(pq)}} I_{on_{state2,(pq)}} t_{off}}{6} \tag{24}$$

The cumulative power losses are determined using the above equation (18) – equation (24). The efficiency can be obtained from equation (25).

$$\eta = \frac{P_{out}}{P_{out}+P_{Loss}} \tag{25}$$

In this part, simulation outcomes for power losses against complex load are compared with conduction and switching losses of a proposed S^2C^2RASCMLI's every switch. From equation (23) and equation (24), the conduction and switching losses are calculated for IGBT as well as diodes in Figure 6. The overall conduction and switch losses are quite low because the reduced active / conduction switch on each mode is only three. H-bridge switches always block the double voltage compare to the input voltage. Switch S_9 losses are very low from the other switches due to the voltage oscillation across the switch is +50V to -50V. Crossed connected switches S_7 / S_8 is conducted only at high voltage levels. S_5 / S_6 switches are conducted for all level of the inverter output voltage as shown in Figure 6.

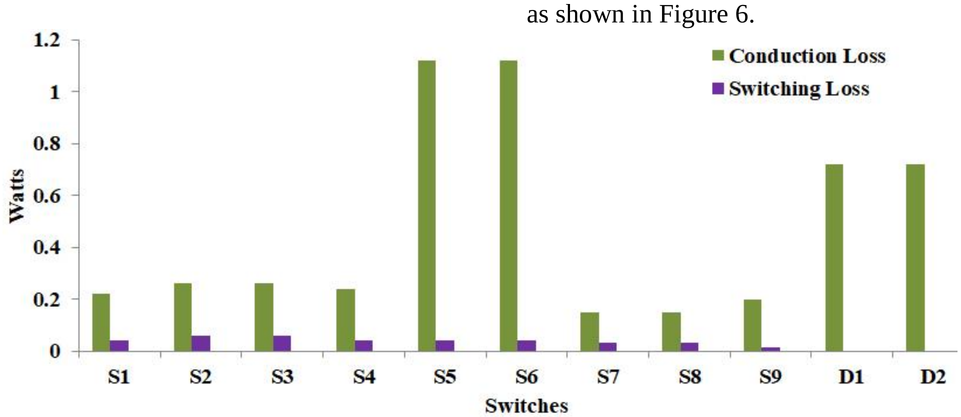

Fig 6 Conduction and switching losses of switches.

7 Comparison of the Proposed S^2C^2RASCMLI with other Topologies

Table 5 Shows the contrast of the suggested S^2C^2RASCMLI with topologies of different kinds based on the number of power electronics switches - N_{IS}, The number of different voltage levels - N_{VL}, The number input - Nv_{in}, Number of flying capacitors - N_C, Number of the switches in conduction path – N_{SC}, Voltage across the capacitors - $V_C(V)$, Total standing voltage of the inverter- $V_{TS}(V)$, Maximum blocking voltage on switches - $V_{BV}(V)$, Number of active devices including diodes - N_{CD}, Maximum output voltage - $V_{o\_max}(V)$, R= $V_{BV}(V)$/ $V_{o\_max}(V)$ (minimum value), the Voltage gain of the inverter, - Ratio of the number of time Discharging and Charging - DC/C (minimum value).

Table 5 shows that the number of conduction switches in the suggested topology is lower than any of the other topologies in the table. Due to these reduced active switches, the power consumption is less and the cost for switches becomes low when compared to another topology. It is the notable advantage of the proposed topologies. The extension HE and VE cells switches have fewer is another advantage of the suggested network. As compared to other proposed circuits, the proposed nine-level S^2C^2RASCMLI has the best overall efficiency and the least amount of loss.

8 Results and Discussion

The title discusses the computation and test results to validate the proposed S^2C^2RASCMLI's performance. Initially, the proposed inverter was simulated in MATLAB/SIMULINK with an input source of 100V and the capacitor of 4700F with a resistance of r_c = 0.124Ω against varying load for fundamental frequency f = 50Hz and switching signal frequency of 5 kHz. The IGBTs (75GB063D) with a ratio of 600V and 75A have a dead time of 4μ seconds from the Driver circuit (TLP250). The load is made up of a variable RL - load with a maximum power rating of 1.25kW.

8.1 Results of the Proposed S^2C^2RASCMLI

Figure 7 depicts the proposed topology's simulation performance.

Table 5 Comparison of the proposed S^2C^2RASCMLI with other topologies.

Ref.	N_{VL}	N_{IS}	N_D	Nv_{in}	N_C	N_{SC}	V_C	V_{TS}	V_{BV}	N_{CD}	V_{o_max}	R	GA	DC/C	$(\eta\%)$
[2]	9	13	-	1	3	7	V_{in}	$25V_{in}$	$4V_{in}$	6	$4V_{in}$	1.0	4.0	3.0	85.9
[9]	9	11	1	1	1	6	V_{in}	$11V_{in}$	$2V_{in}$	4	$2V_{in}$	1.0	2	1.0	96.2
[11]	9	8	4	1	1	4	$2V_{in}$	$16V_{in}$	$4V_{in}$	4	$4V_{in}$	1.0	4	1.0	95.9
[13]	13	16	2	2	4	7	V_{in}	$33V_{in}$	$6V_{in}$	8	$6V_{in}$	1.0	6	2.0	92.1
[14]	9	10	-	1	2	4	$V_{in}/4$	$6V_{in}$	$V_{in}/2$	5	$V_{in}/2$	1.0	0.5	1.0	98.5
[15]	9	12	-	1	1	5	V_{in}	$8V_{in}$	V_{in}	4	V_{in}	1.0	1	1.0	92.3
[16]	5	10	-	1	2	6	V_{in}	$14V_{in}$	$2V_{in}$	4	$2V_{in}$	1.0	2	1.0	94.0
[17]	7	9	1	1	1	4	V_{in}	$16V_{in}$	$2V_{in}$	4	$1.5V_{in}$	1.3	1.5	2.0	97.2
[18]	9	10	1	1	2	4	$V_{in}/2$	$24V_{in}$	$2V_{in}$	2	$2V_{in}$	1.0	2	1.0	95.0
[19]	9	12	-	1	2	7	$V_{in}/2$	$11V_{in}$	V_{in}	4	$2V_{in}$	0.5	2	1.0	80.6
[20]	9	11	-	1	2	6	$V_{in}/2$	$11V_{in}$	V_{in}	4	$2V_{in}$	0.5	2	1.0	NA
[21]	9	12	-	1	2	6	$2V_{in}$	$21V_{in}$	$2\ V_{in}$	5	$4V_{in}$	05	4	1.0	NA
Proposed	9	10	2	1	2	3	$V_{in}/2$	$14V_{in}$	$2\ V_{in}$	5	$2V_{in}$	1	2	1	98.6
Proposed (HE)	13	14	4	1	4	4	$V_{in}/2$	$20V_{in}$	$3V_{in}$	7	$3V_{in}$	.67	3	0.5	97.4
Proposed (VE)	13	14	4	1	4	4	$V_{in}/2$	$20\ V_{in}$	$3\ V_{in}$	7	$3V_{in}$	.67	3	0.5	97.8

NA – Not Available

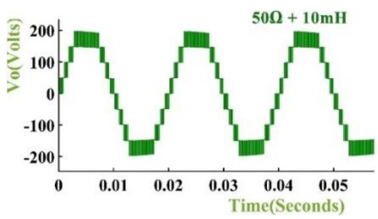

Figure 7(a)

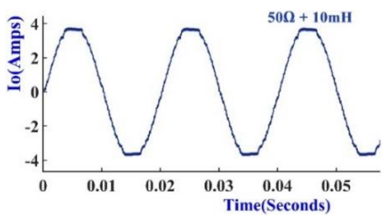

Figure 7(b)

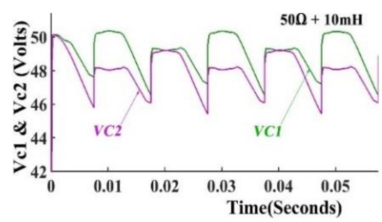

Figure 7(c)

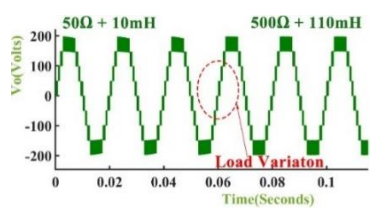

Figure 7(d)

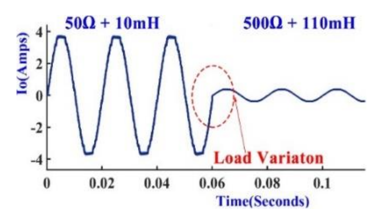

Figure 7(e)

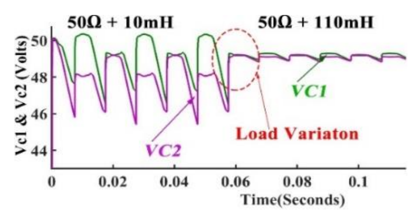

Figure 7(f)

Figure 7(a) voltage at the output – Vo, Figure 7(b) Current at the output - i_o, Figure 7(c) Voltage across the capacitor (V_{C1} & V_{C2}), Figure 7(d) – (f) the voltage and current waveform on load varying condition.

Fig 7 Simulation results of proposed S^2C^2RASCMLI.

Figure 7(a) – Figure 7(c) shows the output voltage and current for R = 50 and L = 10mH. Figure 7 (c) and Figure 7(f) display the voltage around the capacitor in the study and dynamic conditions, respectively. It is observed high ripple in this configuration using capacitors of 4700 µF using capacitors of 4700 microfarads. This adjustment effectively reduces the ripple to below 4%. However, it's important to note that opting for larger capacitors may lead to an increase in the overall weight of the inverter. However, some motor drives or lighting systems, a 10% ripple can be within an acceptable range.

To reaffirm the complex mission, the suggested topology is simulated for load variation from (50Ω + 10mH) to (100Ω + 110mH). The resultant voltage and current waveforms are shown in Figure 7(d) – Figure 7(f). Form this validation; capacitors can maintain the 50V with allowable ripple voltages. In Figure 7 likely includes some form of RL component for smooth start and output filtering, such as a low-pass LC (inductor-capacitor) filter. This LC filter is designed to smooth out the output voltage and current waveforms, making them less prone to rapid fluctuations or ripples.

Figure 8 shows the experimental prototype model. To reduce the inrush current in the capacitor, a small inductor is linked in series with the input supply. The value of the inductor chosen for the loop circuit is determined by the capacitor ripple voltage and device performance.

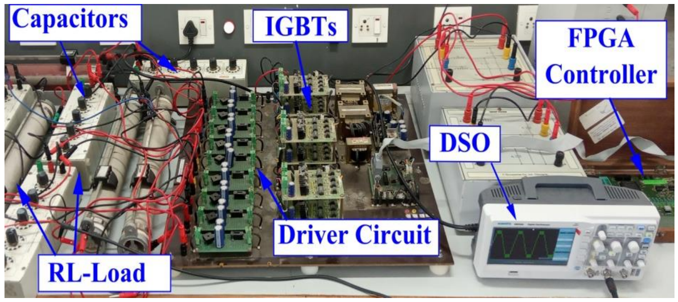

Fig 8 Hardware prototype model.

The proposed S^2C^2RASCMLI topology compare to other recently proposed topologies, the number of active switches and the driver circuits is low. It allows checking circuit connection frequently and improves extended cell operation. In addition, Floating the grounds using diodes can help reduce common-mode voltage, which is often a concern in MLI designs. Common-mode voltage can lead to issues such as electromagnetic interference (EMI).

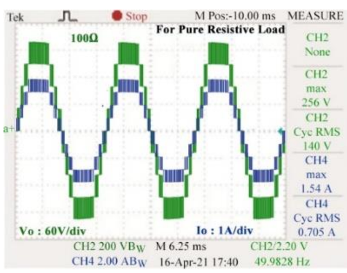

Figure 9(a)

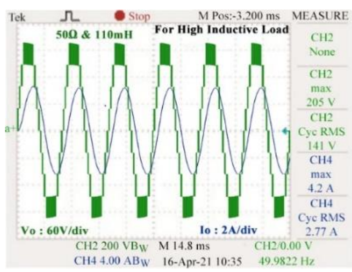

Figure 9(b)

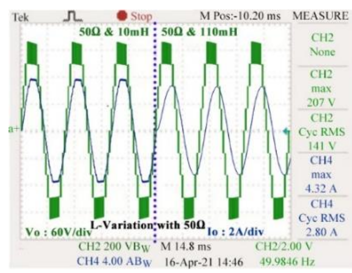

Figure 9(c)

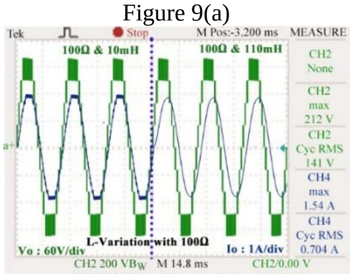

Figure 9(d)

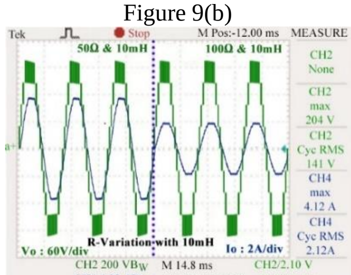

Figure 9(e)

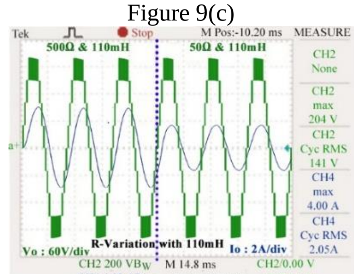

Figure 9(f)

Figure 9(a) Pure Resistive load at 100 Ω, Figure 9(b) RL – load of 110 mH & 50Ω, Figure 9(c) 10 mH to 110 mH with 50Ω resistor, Figure 9(d) 10mH to 110 mH with 100 Ω resistor, Figure 9(e) 50Ω to 100Ω with 10mH, Figure 9(f) 50Ω to 100Ω with 110mH.

Fig. 9 Experimental output voltage and current waveforms at fixed and dynamic load condition.

Figure 9 depicts the proposed inverter's voltage and current waveforms with varied inductor and resistor loads in a dynamic scenario. Figure 9(a) shows a purely resistive load with voltage and in-phase current and the smooth sinusoidal current waveform generated by an inverter with a high inductance value. It is shown in Figure 9(b).

The twice voltage gain as shown by the output voltage is one of the key features of the proposed topology, which has a 200V peak resulting from the 100V_{in}. Further, Figure 9(c) – Figure 9(f) shows the output voltage and current on various dynamic load conditions.

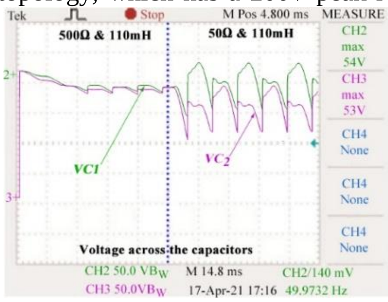

Figure 10(a)

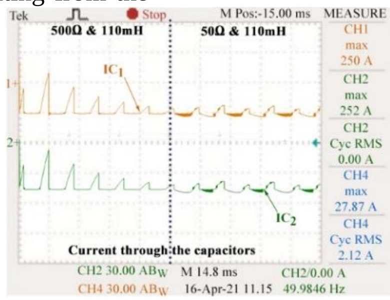

Figure 10(b)

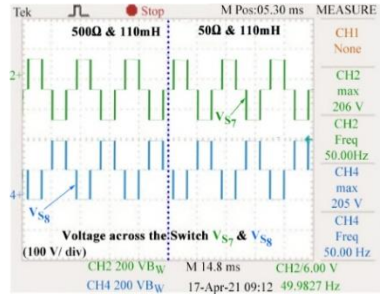

Figure 10(c)

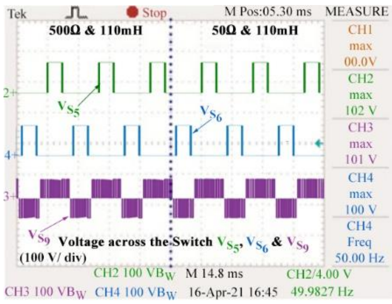

Figure 10 (d)

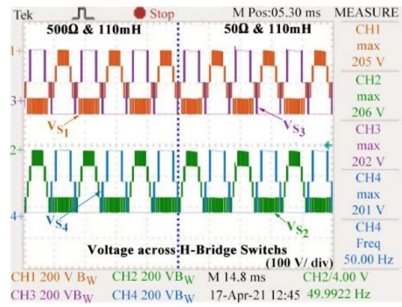

Figure 10 (e)

Figure 10(a) voltage across the capacitor, Figure 10(b) Current through the capacitors, Figure 10(c) voltage stresses on V_{S7} & V_{S8}, Figure 10(d) voltage stresses on V_{S5}, V_{S6} & V_{S9}, Figure 10(e) voltage stresses on H- bridge switches V_{S1}, $V_{S2,}$ V_{S3} & V_{S4}.

Fig. 10 The capacitor voltage, current and voltage stress of the switches at the dynamic load condition.

Figure 10 shows the voltage and current at different components in the proposed nine-level S^{2}C^{2}RASCMLI at the dynamic variation of loading conditions of 500Ω + 110mH to 50Ω + 110mH. The balanced capacitor voltage and current waveforms are shown in Figure 10(a) and Figure 10(b) respectively. Both capacitor voltages V_{c1} and V_{c2} are equally distributed and equal to half of the V_{in}. The voltage across the switches on RL dynamic load is shown in Figure 10(c) – Figure 10(e) at an input voltage of 100V. Furthermore, at an output power of 400W and a fundamental frequency of 50Hz, the proposed inverter's efficiency has been estimated to be 98.6%. All of these findings show that the proposed nine-level S^{2}C^{2}RASCMLI topology is sustainable and feasible under different load varying conditions.

8.2 Result of the Proposed 13-Level S^{2}C^{2}RASCMLI (HE & VE)

The performance of the suggested 13-Level S^{2}C^{2}RASCMLI is addressed in this chapter. The horizontal and vertical extension topology simulation waveforms are shown in Figure 11(a) – (f) at f = 50 Hz under dynamic RL –Load.

Although experimental results of horizontal and vertical extension inverter waveforms are shown in Figure 13. Figure 13(a) – Figure 13(d) demonstrating the feasibility of the suggested extension network and shows the output voltage, current and voltage across the capacitors under dynamic load variation.

From the extension operation, the long-time charging capability of capacitors increases the performance of the inverter particularly at the low voltage boosting. However, the proposed vertical extension topology has a better performance compared to the horizontal extension as per the voltage ripple factor of the capacitor as shown in Figure 12(b) and Figure 12(d). As per the calculation, the maximum efficiency of horizontal and vertical extension topologies is 97.4% and 97.8% respectively on a load of (50Ω + 110mH).

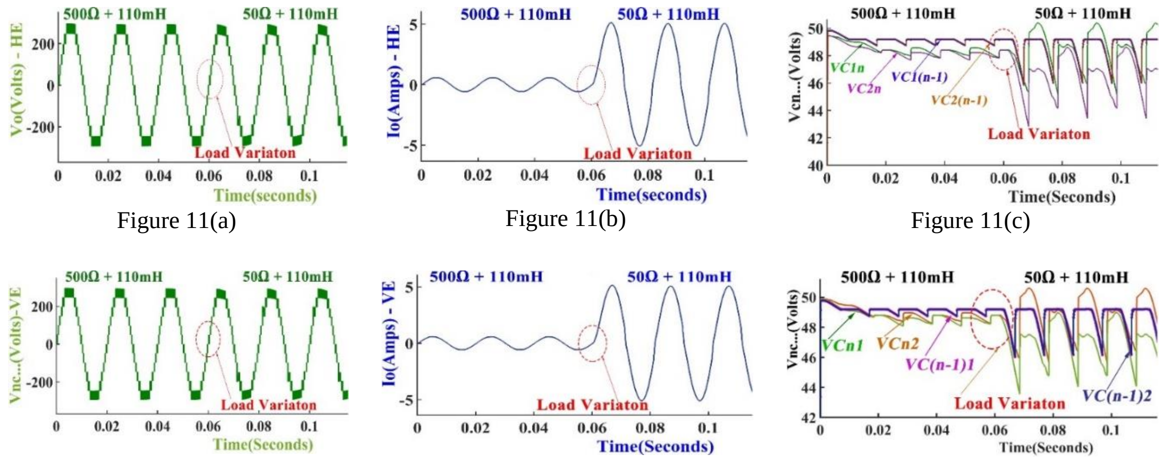

Figure 11(a) Figure 11(b) Figure 11(c)

Figure 11(d) Figure 11(e) Figure 11(f)

Figure 11(a) Voltage at the output, Figure 11(b) current at the output, Figure 11(c) voltage across the capacitor at dynamic load conditions of horizontal extension. Similarly Figure 11(d) – (f) output voltage, current and voltage across the capacitor of the vertical extension.

Fig. 11 Waveforms of the proposed 13-Level S^2C^2RASCMLI in simulation.

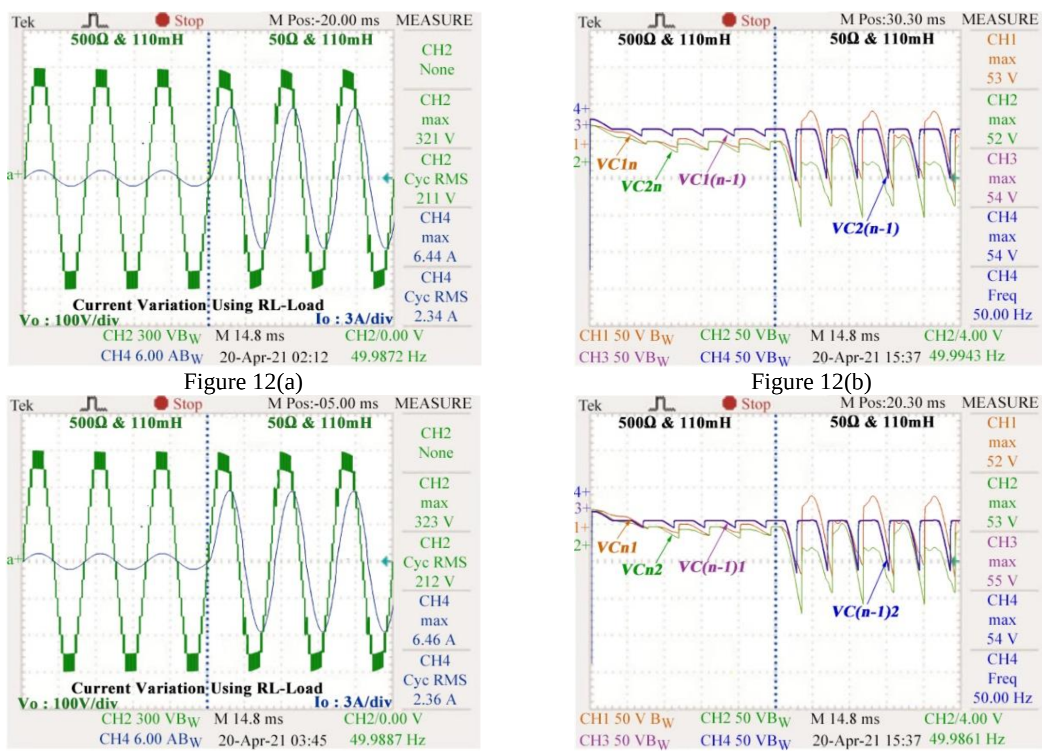

Figure 12(a) Figure 12(b)

Figure 12(c) Figure 12(d)

Figure 12(a) Waveforms of output voltage and current (HE), Figure 12(b) voltage across the capacitors (HE), Figure 12(c) Waveforms of output voltage and current (VE), Figure 12(d) voltage across the capacitors (VE).

Fig. 12 Experimental output voltage and current waveforms of the 13-level inverter.

9 Conclusion

This paper proposes a new nine-level S^2C^2RASCMLI topology. The proposed nine-level boost inverter topology is based on a switched-capacitor with fewer active switches. The proposed topology shoes that in conditions of reduced active component needs for the same number of voltage levels is highlighted in a comprehensive comparative study. Furthermore, the proposed S^2C^2RASCMLI is expanded to n levels and serves as the foundation for the proposed Horizontal or Vertical extensions. A formalized switching table is given for further processing in the proposed extension inverter. The results of simulations and experiments presented here have confirmed the proposed topology's ability to manage a variety of loading conditions. Finally, the extensive relative study confirmed the qualities of the proposed topology and demonstrating its feasibility for a variety of applications, especially in renewable energy sources at dynamic load conditions.

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