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Research Paper

High Step-Up Interleaved DC/DC Converter Using VM Cell for PV Applications

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Abstract: This work proposes a high step-up interleaved dc/dc topology utilizing a VM (voltage multiplier) cell suitable for PV applications. The VM cells D/C (Diode/Cap.) are cascaded among the phases to approach a high voltage gain. Besides, the voltage converting ratio of the presented structure can be improved by extending the VM cells and it also leads to drop in the normalized voltage stress throughout the switches and some diodes. Therefore, by utilizing a semiconductor (Switch/Diode) with a lower rating leads to a decline in system losses. Also, the efficiency of the suggested topology will be considerable and the overall cost can be decreased. To elaborate on the main benefits of the proposed topology, a comparison has been made across other literature regarding the efficiency, peak voltage throughout the semiconductors and voltage ratio of the converter. To prove the accuracy principle of operation of the suggested converter, two prototypes (for n=1, 2 stages) were built and tested at 350 W and 453 W with an operating frequency of about 40 kHz performed.

Keywords: DC/DC Converter, Voltage Multiplier Cell, High Step-Up, Interleaved, Low Voltage Stress.

1 Introduction

NOWDAYS, power converters with high voltage converting ratio have been developed in different applications. Generally, the output voltage of sustainable sources is not high. A high gain dc-dc structure should be utilized to solve the mentioned issue. Therefore, dc-dc converters use various techniques for solving the mentioned issues of renewable sources and EV applications which these techniques consist of a transformer, voltage multiplier cell (diode-capacitor, coupled-inductor, diode-capacitor-inductor) and cascade converters [1-6].

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Since conventional boost converters have static problems at high power levels and large duty cycle values, advanced dc-dc converters with the aforementioned techniques should be utilized among the renewable resources and grid. It causes to evaluate the operation of dc-dc topologies in large duty cycle values and to decrease the normalized voltage stresses across MOSFETs [6]. Efficiency and operation quality of the converters are influenced by switching in high duty cycles. Related to voltage gain equations of the conventional converters, they should convert the input to high voltage. However, issues like inductor resistance effect, converter loss and voltage drop on semiconductors limit operations at high duty cycle values. Generally, isolated type of converters is usable in the cases that isolating is obligatory [7]. The voltage gain is affected by the turn's ratio value of the transformer. Nevertheless, the leakage inductance related to transformer certainly induces intensive disadvantages, such as voltage oscillation.

Thus, capacitor/diode clamping and absorbing cells (VM) should be applied which leads to the complexity of the circuit topology and limited overall efficiency [8]. However, dc-dc non-isolated converters have no problems with dc-dc isolated converters. Todays, dc-dc non-isolated converters with voltage multiplier units are used more in renewable applications. [9, 10]. As the number of voltage multiplier units increase, the used power components of the converter will be increased, which causes the structure to be complex. However, the power semiconductors (Diode/Switch) are clamped by capacitors of VM units, so the onomastic value of D/Cs will be limited at high power rating. [11]. Consequently, the rating of used power semiconductors has been decreased and the overall cost of the system will be improved. Furthermore, to achieve a large gain by converter, the coupled inductor techniques can be useful and appropriate turns ratio will increase the gain further. However, a snubber circuit needed to envelop the energy stored in the leakage inductor. Generally, it leads to complexity of the structure and high-power losses. [12, 13].

The voltage multiplier cell (VMC) is an efficient and inexpensive simple topology that typically includes a diode/capacitor to achieve a large voltage level at output. Applying a VMC with a small inductance added to the boost converter can obtain lower losses and zero current switching (ZCS) on semiconductors, thereby greatly limiting losses and augmenting overall efficiency. The high step-up structure will exist by adding voltage multiplier units with conventional boost structures [14-17]. In this work, an ultra-boost dc-dc topology using VM techniques is presented for sustainable energies. The presented topology uses interleaved techniques and diode/capacitor units for achieving a high voltage gain and significant overall efficiency. The semiconductors are clamped by capacitors of VM units, so they make use of lower rating diodes and switches. Besides, by utilizing a switch with lower conducting resistance, the overall system losses can be reduced.

2 Proposed structure and operation principle

Fig.1 depicts the circuit of the presented topology. The presented topology is a transformer-less high voltage gain interleaved dc/dc structure that includes dc power supply as a input, an interleaved structure with four phases, four power MOSFETs, four inductors, each of them are series in one phase and VM cells (diode/capacitor). Each VM cell contains five capacitors/diodes that are connected between the up and down phases, symmetrically. This work causes to create an equal voltage for up and down section capacitors. Generally, all number of components in each VM cell for each section (up/down) is 5, then the number for the up/down section is 10. The sum of D/C is 2n+3, which is the number of stages (k=1,2, 3, …, n). Voltage gain of the recommended topology could be improved by higher VM stages. Also, the maximum voltage of semiconductors (switches/diodes) can be decreased with this method. The power level of the presented structure can be risen by promoting the current level and voltage level between the phases in which this work is possible by adding VM cells. Besides, the input current ripple of the presented structure will decrease due to the use of the interleaved techniques. Generally, the proposed structure is capable to obtain high voltage with lower losses in the semiconductors. Also, having lower input current ripple makes the presented structure considered as a good choice for the green sources.

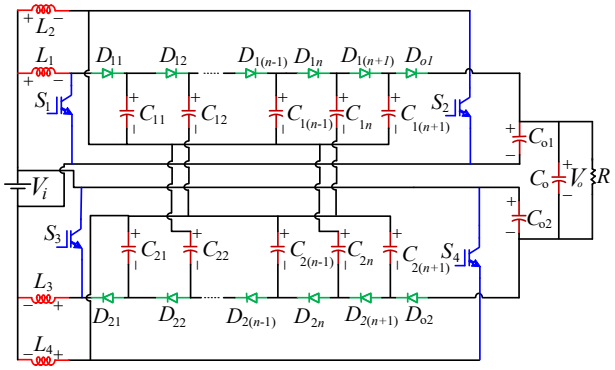


Fig. 1 Presented structure

3 Proposed structure analysis

Theoretical analysis of the suggested topology and equivalent circuits in one period in CCM (continuous conduction mode) operation are obtained in this part. Generally, to simplicity the operation of technical survey, some presumptions are carried out as:

- The input power source is unchangeable and consider constant,
- All components are assumed to be ideal,
- The voltage ripple of capacitors is considered equal to zero due to the large capacity value.

$$L_1 = L_2 = L_3 = L_4$$

$$C_{11} = C_{21}, C_{12} = C_{22}, C_{13} = C_{23},$$

$$C_{14} = C_{24}, \ldots, C_{1n} = C_{2n}, C_{o1} = C_{o2}$$

The analysis of the different modes of the recommended structure in CCM for each switching period (Ts) of one switch can be described as a two-operation time interval. DTs are the first operation time in which the power switch is conducted and (1-D)Ts is the second time interval in which the power switch is OFF. The recommended converter has an eight-time interval in CCM operation, which are indicated in Figs. 2 and 3. Then, these modes could be analyzed as:

Mode 1 [$t_0 = 0 \le t \le t_1 = (D - \frac{1}{2})T_s$ **]:**

$S_{1,2,4}$ are conducting and S_3 is turned off. Also, all diodes in up section (D_{11}, D_{12}, …, D_{1n}, $D_{1(n+1)}$, D_{o1} are turned-off. In the down section, diodes D_{21}, D_{23}, …, $D_{2(n+1)}$, D_{o2} are turned-on and diodes D_{22}, D_{24},…, D_{2n} are blocked. The inductors L_1, L_2 and L_4 receive their energy from the input power resources, then the inductors current of L_1, L_2 and L_4 will increase. The stored energy of L_3 is forwarded to C_{23}, C_{25}, …, $C_{2(n-1)}$, $C_{2(n+1)}$, C_{o1} and C_{o2}, then the inductor L_3 current is linearly declined. By noticing the equivalent circuit can be written as:

$$V_{L1} = V_{L2} = V_{L4} = V_i \quad (1)$$

$$V_{L3} = V_i - V_{C21} \quad (2)$$

$$\begin{cases} V_{C2k} = V_{C2(k-1)} + V_i \\ k = 3,5,7,...,n+1 \end{cases} \quad (3)$$

$$V_{D11} = V_{C11} \quad (4)$$

$$\begin{cases} V_{D1k} = V_{C1(k-1)} - V_i - V_{C1k} \\ k = 2,4,6,...,n \end{cases} \quad (5)$$

$$\begin{cases} V_{D1k} = V_i + V_{C1(k-1)} - V_{C1k} \\ k = 3,5,7,...,n,n+1 \end{cases} \quad (6)$$

$$V_{Do1} = V_{C1(n+1)} - V_{Co1} \quad (7)$$

$$\begin{cases} V_{D2k} = V_{C2(k-1)} - V_i - V_{C2k} \\ k = 2,4,6,...,n \end{cases} \quad (8)$$

$$V_{Do2} = V_{C2n} + V_i - V_{Co2} \quad (9)$$

$$V_{S3} = V_{C21} \quad (10)$$

Mode 2 [$t_1 = (D - \frac{1}{2})T_s \le t \le t_2 = \frac{T_s}{4}$ **]:**

The power switches S_1, S_4 remains in ON-state and the switches S_2, S_3 are switched off. Diodes D_{12}, D_{14}, …, D_{1n}, D_{o1} in up-section and diodes D_{21}, D_{23},…, $D_{2(n-1)}$, D_{o2} are conducting and other diodes are blocked. The inductors L_1 and L_4 receive their energy from the DC supply. The stored energy of L_2 is forwarded to C_{11}, C_{13}, …, $C_{1(n-1)}$, $C_{1(n+1)}$, C_{o1} and the stored energy of L_3 is forwarded C_{23}, C_{25}, …, $C_{2(n-1)}$, $C_{2(n+1)}$, C_{o1} and C_{o2}. Thus, the inductors L_2 and L_3 current is reduced linearly. Related to Fig. 2(b), the follows equations is given:

$$V_{L1} = V_{L4} = V_i \quad (11)$$

$$V_{L2} = V_i + V_{C1(n+1)} - V_{Co1} \quad (12)$$

$$V_{L3} = V_i - V_{C21} \quad (13)$$

$$\begin{cases} V_{D1k} = V_{C1(k-1)} + V_{C2k} - V_{C1k} - V_{C2(k-1)} \\ k = 3,5,7,...,n+1 \end{cases} \quad (14)$$

$$\begin{cases} V_{D2k} = V_{C2(k-1)} + V_{Co1} - V_{C1(k+1)} - V_{C2k} - V_i \\ k = 2,4,6,...,n \end{cases} \quad (15)$$

$$V_{S2} = V_{Co1} - V_{C1(n+1)} \quad (16)$$

Mode 3 [$t_2 = \frac{T_s}{4} \le t \le t_3 = (D - \frac{1}{4})T_s$ **]:**

In this time instant, $S_{1,3,4}$ are in ON-state and S_2 is OFF. Diodes D_{11}, D_{13}, …, $D_{1(n+1)}$ and all diodes in the down section are blocked. The inductors L_1, L_3 and L_4 receive their energy from the input DC supply and the stored energy of L_2 is forwarded to C_{21}, C_{22}, …, $C_{2(n-1)}$, $C_{2(n+1)}$. Thus, current of L_1, L_3 and L_4 are linearly raised and the inductor L_2 current is decreased. Using Fig. 2(c), we have the following equations:

$$V_{L1} = V_{L3} = V_{L4} = V_i \quad (17)$$

$$V_{L2} = V_i + V_{C1(n+1)} - V_{Co1} \quad (18)$$

Mode 4 [$t_3 = (D - \frac{1}{4})T_s \le t \le t_4 = \frac{T_s}{2}$ **]:**

This mode start when S_1, S_3 are switched on and S_2, S_4 are off. Diodes D_{11}, D_{13}, …, $D_{1(n+1)}$ in up section and D_{21}, D_{23}, …, $D_{2(n+1)}$ are blocked and other diodes are conducting. L_1 and L_3 receive their energy from power supply, then these inductors current is linearly raised. The inductors L_2 and L_4 forwarded their stored energy to the capacitors C_{o2} and C_{o1}, respectively. The follows equations are applied to this operation time:

$$V_{L1} = V_{L3} = V_i \quad (19)$$

$$V_{L2} = V_i + V_{C1(n+1)} - V_{Co1} \quad (20)$$

$$V_{L4} = V_i + V_{C2(n+1)} - V_{Co2} \quad (21)$$

$$V_{S4} = V_{Co2} - V_{C2(n+1)} \quad (22)$$

$$\begin{cases} V_{C2k} + V_{C1(k-1)} = V_{C1k} + V_{C2(k-1)} \\ k = 2,4,6,...,n \end{cases} \quad (23)$$

Mode 5 [$t_4 = \frac{T_s}{2} \le t \le t_5 = DT_s$ **]:**

In this time interval, the power switches S_1, S_2, S_3 are conducting and S_4 is switched off. Diodes D_{11}, D_{13}, …, $D_{1(n-1)}$ in up section and diodes D_{21}, D_{23},…, $D_{2(n-1)}$ in the down section are off and other diodes are on. The inductors L_1, L_2 and L_3 receive their energy from the input dc power source and the stored energy in L_4 is transferred to C_{o1} and C_{o2}. Using Fig. 3(a), we have:

$$V_{L1} = V_{L2} = V_{L3} = V_i \quad (24)$$

$$V_{L4} = V_i + V_{C2(n+1)} - V_{Co2} \quad (25)$$

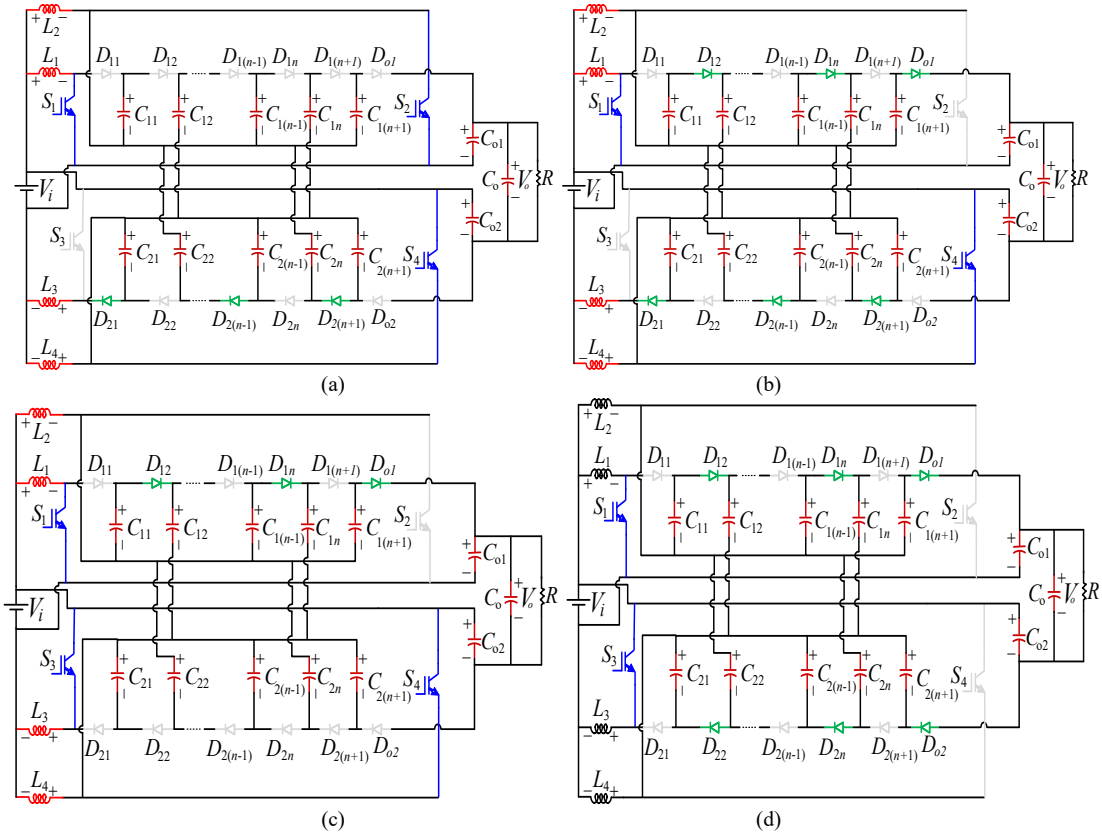


Fig. 2 The operation modes of the suggested topology in CCM.

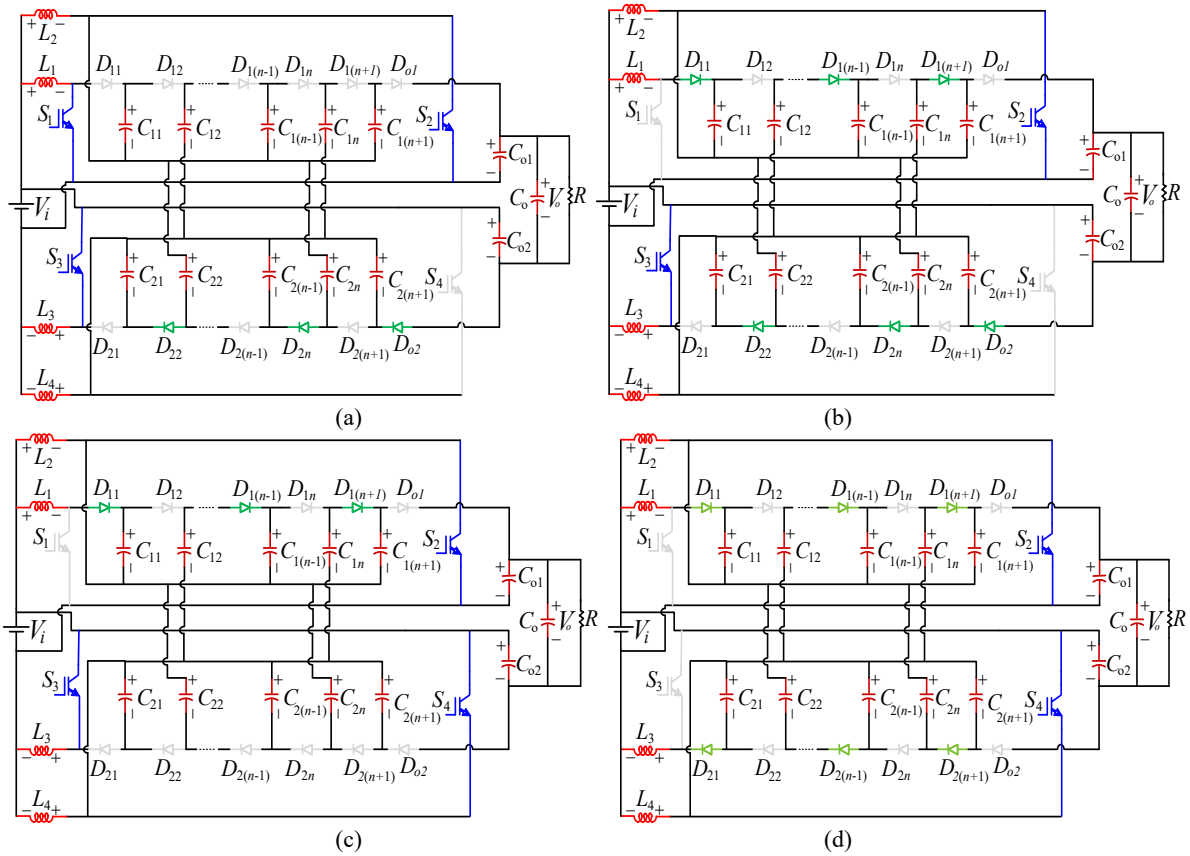


Fig. 3 The operation modes of the recommended structure in CCM.

Mode 6 [$t_5 = DT_S \le t \le t_6 = \frac{3}{4}T_S$]:

S_2, S_3 are ON and S_1, S_4 are OFF. Diodes D_{12}, D_{14}, …, D_{1n}, D_{o1} in up-section and diodes D_{21}, D_{23}, …, $D_{2(n+1)}$ are turned-off and other diodes are ON. The inductors L_2 and L_3 receive their energy from the power source. The stored energy in L_1 and L_4 are forwarded to C_{21}, C_{23}, …, $C_{2(n\text{-}1)}$, $C_{2(n+1)}$, C_{o2} and C_{11}, C_{13}, …, $C_{1(n\text{-}1)}$, $C_{1(n+1)}$, C_{o1}, respectively. The inductors L_1 and L_4 current are linearly decreased. Regarding Fig. 3(b), can be written as:

$$V_{L1} = V_i + V_{C11} \tag{26}$$

$$V_{L2} = V_{L3} = V_i \tag{27}$$

$$V_{L4} = V_i + V_{C2(n+1)} - V_{Co2} \tag{28}$$

$$V_{S2} = V_{Co} + V_i + V_{C11} - V_{Co1} - V_{Co2} \tag{29}$$

Mode 7 [$t_6 = \frac{3}{4}T_S \le t \le t_7 = (D + \frac{1}{4})T_S$]:

In this time instant, The power switches, S_2, S_3 and S_4 are conducting and S1 is switched OFF. Diodes D_{12}, D_{14}, …, D_{1n}, D_{o1} in the up section and all diodes in the down section are blocked. The inductors L_2, L_3, L_4 receive their energy from the DC source, then the inductors current is raised. The current of the inductor L_1 is decreased. The capacitors C_{o1}, C_{o2} are charged by the inductor L_1 storing energy in. Regarding Fig. 3(c), we have:

$$V_{L1} = V_i - V_{C11} \tag{30}$$

$$V_{L2} = V_{L3} = V_{L4} = V_i \tag{31}$$

Mode 8 [$t_7 = (D + \frac{1}{4})T_S \le t \le t_8 = T_S$]:

In this time interval, the power MOSFETS S_2, S_4 are ON and S_1, S_3 are OFF. Diodes D_{12}, D_{14}, …, D_{1n}, D_{o1} in up section and D_{22}, D_{24}, …, D_{2n}, D_{o2} in the down section are blocked. The inductors L_2 and L_4 receive their energy from the input DC source, then the current of these inductors is linearly raised. The inductors L_1 and L_3 currents are linearly reduced. The C_{22}, C_{24}, …, C_{2n}, C_{o2} are charged via the storing energy in the L_1 and the capacitors C_{21}, C_{23}, …, $C_{2(n\text{-}1)}$, $C_{2(n+1)}$ are charged by the stored energy in the L_3, respectively.

$$V_{L1} = V_i - V_{C11} \tag{32}$$

$$V_{L2} = V_{L4} = V_i \tag{33}$$

$$V_{L3} = V_i - V_{C21} \tag{34}$$

Considering the volt-second principle for the inductors $L_{1\text{-}4}$ (the average voltage across each of inductors is zero in switching period), the capacitors voltage based on D can be defined as:

$$\begin{cases} V_{C1k} = \dfrac{k}{1-D} V_i \\ k = 1,3,\ldots,n+1 \end{cases} \tag{35}$$

$$\begin{cases} V_{C1k} = \dfrac{k+1-2D}{1-D} V_i \\ k = 2,4,6,\ldots,n \end{cases} \tag{36}$$

$$\begin{cases} V_{C2k} = \dfrac{k}{1-D} V_i \\ k = 1,,3,\ldots,n+1 \end{cases} \tag{37}$$

$$\begin{cases} V_{C2k} = \dfrac{1+k-2D}{1-D} V_i \\ k = 2,4,6,\ldots,n \end{cases} \tag{38}$$

$$V_{C(o1)} = V_{C(o2)} = \frac{n+3-D}{1-D} V_i \tag{39}$$

Considering the KVL principle for Fig. 1, the following equation are expressed:

$$V_o = V_{Co1} + V_{Co2} - V_i \tag{40}$$

Using (39) and (40), the ratio of the voltage conversion of the recommended converter in CCM (M_{CCM}) is defined as follows:

$$\begin{cases} M_{CCM} = \dfrac{V_o}{V_i} = \dfrac{5+2k-D}{1-D} \\ k = 1,2,3,\ldots,n \end{cases} \tag{41}$$

Where k is the number of stages of the VM cells.

Based on (41), the voltage gain of the presented topology is high and the increasing of the voltage gain can be realized by extending the stages of VM cells. Also, the normalized voltage stress through the diodes and switches of circuit will be decreased by adding the number of VM stages.

The maximum voltage stress of the switches is achieved as follows:

$$\begin{cases} \left|\dfrac{V_{Switch}}{V_o}\right| = M_{S1} = M_{S3} = \dfrac{M_{CCM}-1}{(4+2k)M_{CCM}} \\ \left|\dfrac{V_{Switch}}{V_o}\right| = M_{S2} = M_{S4} = \dfrac{M_{CCM}+3+2k}{(4+2k)M_{CCM}} \end{cases}, \quad k = 1,2,\ldots,n \tag{42}$$

Also, the peak voltage throughout the power diodes can be given by following equations:

$$\left|\frac{V_{D11}}{V_o}\right| = \left|\frac{V_{D21}}{V_o}\right| = \frac{M_{CCM}-1}{(4+2k)M_{CCM}} \tag{43}$$

$$\begin{cases} \left|\dfrac{V_{D1k}}{V_o}\right| = \left|\dfrac{V_{D2k}}{V_o}\right| = \dfrac{M_{CCM}+3+2k}{(4+2k)M_{CCM}} \\ k = 2,4,\ldots,n \end{cases} \tag{44}$$

$$\begin{cases} \left|\dfrac{V_{D1k}}{V_o}\right| = \left|\dfrac{V_{D2k}}{V_o}\right| = \dfrac{M_{CCM}-5-2k}{(4+2k)M_{CCM}} \\ k = 3,5,\ldots,n+1 \end{cases} \tag{45}$$

$$\left|\frac{V_{Do1}}{V_o}\right| = \left|\frac{V_{Do2}}{V_o}\right| = \frac{3M_{CCM}-16-4k}{(4+2k)M_{CCM}} \tag{46}$$

3.1 Components current calculation

Considering the current-second principle for capacitors in single switching interval (the average current flowing through the capacitors are equal to zero in one switching cycle), it can be mentioned that the diodes average current is equivalent to the output average current:

$$\begin{cases} I_{D1k} = I_{D2k} = I_{Do1} = I_{Do2} = I_o \\ k = 1,2,...,n \end{cases} \quad (47)$$

Generally, by applying KCL law in Fig. 1, the following relations can be expressed:

$$I_i = I_{S1} + I_{S2} + I_{L3} + I_{L4} \quad (48)$$

$$I_i = I_{S3} + I_{S4} + I_{L1} + I_{L2} \quad (49)$$

The input and output current relationship can be obtained by using (41) as follows:

$$I_i = \frac{5 + 2k - D}{1 - D} I_o \quad (50)$$

With regard to Fig. 1, by performing the current-second principle across the power diodes, the switches average current is calculated by:

$$I_{S1} + I_{S2} = I_{S3} + I_{S4} = \frac{k+2}{1-D} I_o \quad (51)$$

$$\begin{cases} I_{S1} = I_{S3} = \frac{2+k}{5(1-D)} I_o \\ I_{S2} = I_{S4} = \frac{4(2+k)}{5(1-D)} I_o \end{cases} \quad (52)$$

The average current of the inductors is achieved as follows:

$$I_{L1} + I_{L2} = I_{L3} + I_{L4} = \frac{3 + k - D}{1 - D} I_o \quad (53)$$

$$\begin{cases} I_{L1} = I_{L3} = \frac{5(3+k-D)}{16(1-D)} I_o \\ I_{L2} = I_{L4} = \frac{11(3+k-D)}{16(1-D)} I_o \end{cases} \quad (54)$$

Fig. 4 illustrates the basic waveforms of the proposed structure in continuous conduction mode.

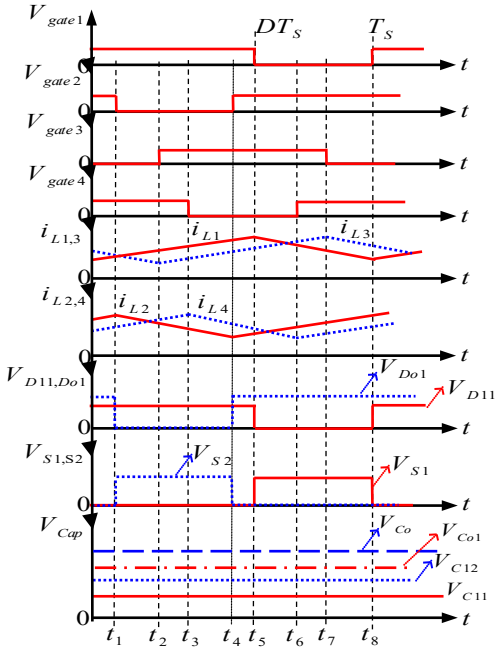


Fig. 4 The basic waveforms of recommended topology in CCM operation

3.2 Efficiency calculation

For analysis of the system efficiency of the recommended dc-dc topology ($\eta_{Converter}$), the power components parasitic elements are carried out as follows:

- $R_{DS-on} \rightarrow$ conducting resistance of the active switch,
- r_{L1}, r_{L2}, r_{L3}, $r_{L4} \rightarrow$ the each inductor (L_1, L_2, L_3 and L_4), equivalent series resistance (ESR),
- r_{D11}, r_{D12},…, $r_{D1(n+1)}$, r_{Do1}, r_{D21}, r_{D22} ,…, $r_{D2(n+1)}$, r_{Do2} are ESR of diodes,
- $r_C \rightarrow$ ESR of the capacitors,

Generally, the overall efficiency of the recommended dc-dc structure is defined as follows:

$$\eta_{Conv.} = \frac{P_o}{P_o + P_{losses}} \times 100\% \quad (55)$$

Since the overall loss of the active switch is consisted of the switching period losses and conduction interval losses, then the total power losses of the active switches can be formulized as follows:

$$\begin{cases} P_S = P_{R_{DS-ON}} + \frac{1}{2} P_{Switching} \\ = \frac{2}{25} R_{DS-ON} \times I_o^2 [(\frac{2+k}{1-D})^2 + (\frac{4(2+k)}{1-D})^2] + 2C_S (\frac{V_i}{1-D})^2 f_S \end{cases} \quad (56)$$

The conduction losses of the magnetic components are given in the following:

$$\begin{cases} P_{L_1,L_2,L_3,L_4} = \sum_{j=1}^{4} (r_{L_j} \times I_{L_{j(rms)}}^2) \\ = 2r_{L_{1,3}} \left[\frac{5(3+k-D)}{16(1-D)} I_o \right]^2 + 2r_{L_{2,4}} \left[\frac{11(3+k-D)}{16(1-D)} I_o \right]^2 \end{cases} \quad (57)$$

The voltage drop losses ($P_{VF_{(Diodes)}}$) and conduction losses ($P_{RF_{(Diodes)}}$) of the power diodes is expressed by:

$$\begin{cases} P_{Losses_{(Diodes)}} = P_{RF_{Djk}} + P_{VF_{Djk}} \\ = r_{F_{Djk}} \times (\frac{I_o}{1-D})^2 + V_{F_{Djk}} \times (\frac{I_o}{1-D}) \\ j = 1,2 \;\&\; k = 1,2,...,n+2 \end{cases} \quad (58)$$

The capacitors total losses is written as follows:

$$\begin{cases} P_{Losses\,(Cap.)} = \left[\sum_{k=1}^{n+1} (r_{R_{C1k}} \times I_{R_{C1k(rms)}}^2) + \sum_{k=1}^{n+1} (r_{R_{C2k}} \times I_{R_{C2k(rms)}}^2) \right] \\ + \left[(r_{R_{Co1}} \times I_{R_{Co1(rms)}}^2) + (r_{R_{Co2}} \times I_{R_{Co2(rms)}}^2) \right] + (r_{R_{Co}} \times I_{R_{Co(rms)}}^2) \end{cases} \quad (59)$$

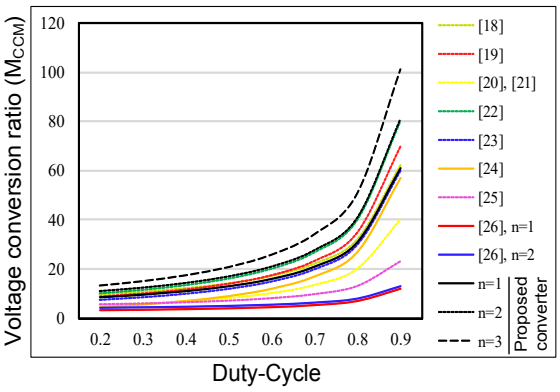
Using (57)-(69), the total efficiency of the recommended structure can be found as:

$$\begin{cases} \eta_{Converter} = \frac{P_o}{P_o + P_{losses}} \times 100\% \\ P_{losses} = L_1 + L_2 + L_3 + L_4 + L_5 \\ L_1 = \frac{2}{25} R_{DS-ON} \times I_o^2 [(\frac{2+k}{1-D})^2 + (\frac{4(2+k)}{1-D})^2] + 2C_S (\frac{V_i}{1-D})^2 f_S \\ \begin{cases} L_2 = V_{F_{Djk}} \times (\frac{I_o}{1-D}) \\ j = 1,2 \;\&\; k = 1,2,...,n+2 \end{cases} \\ \begin{cases} L_3 = r_{F_{Djk}} \times (\frac{I_o}{1-D})^2 \\ j = 1,2 \;\&\; k = 1,2,...,n+2 \end{cases} \\ L_4 = 2r_{L_{1,3}} \left[\frac{5(3+k-D)}{16(1-D)} I_o \right]^2 + 2r_{L_{2,4}} \left[\frac{11(3+k-D)}{16(1-D)} I_o \right]^2 \\ L_5 = \left[\sum_{k=1}^{n+1} (r_{R_{C1k}} \times I_{R_{C1k(rms)}}^2) + \sum_{k=1}^{n+1} (r_{R_{C2k}} \times I_{R_{C2k(rms)}}^2) \right] \\ + \left[(r_{R_{Co1}} \times I_{R_{Co1(rms)}}^2) + (r_{R_{Co2}} \times I_{R_{Co2(rms)}}^2) \right] + (r_{R_{Co}} \times I_{R_{Co(rms)}}^2) \end{cases} \quad (60)$$

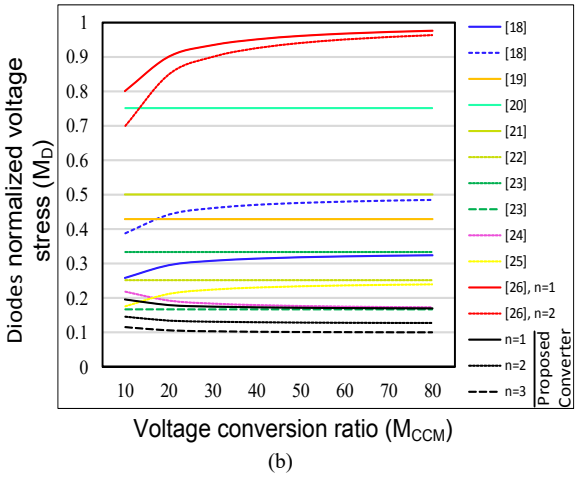
4 Comparison results

In this part of the paper a comparison has been made, in terms of MCCM, MS, MD, No. of diode, No. of switch, No. of capacitor, No. of inductor and the number of VM steps is presented. To compare the normalized maximum voltage through the semiconductors (MOSFET/Diode) among the presented topology and other topologies, N is considered as 2. Fig. 5(a) presents the collation of voltage gain at introduced converter and several other structures in continuous conduction mode (MCCM) in terms of duty cycle value (D). These curves are provided by k=1, 2.

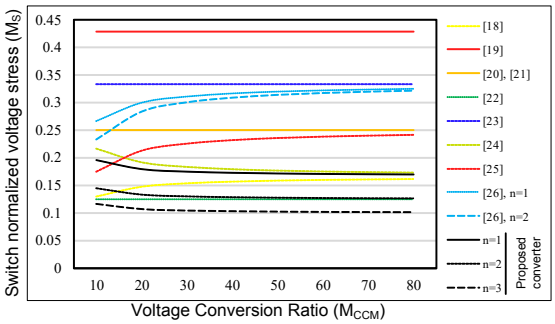
According to the curves, it is noteworthy that the voltage gain of the presented topology enhances by growth of the number of stages. Also, the voltage enhancement ratio of the suggested converter is remarkable in comparison to the others in [20, 21]. In conclusion, the suggested structure could be considered as a high voltage gain DC-DC converter. Nevertheless, parasitic components cause the limitation of the generated voltage of the converter and this notion affects the total efficiency of the system. Possessing a high voltage converting ratio converter utilizing a lower number of components leads to a reduction of losses.



(a)



(b)



(c)

Fig. 5. Comparison between the suggested structure and other structures,
(a) Variations of voltage gain various duty cycles,
(b) Variations of switches normalized peak voltage based on voltage gain,
(c) Variations of diodes normalized peak voltage based on voltage gain,

Fig. 5(b) is related to the voltage of the main power switch in the presented converter. It can be deduced from the figure that the normalized peak voltage value on the switches of the recommended converter has lower values and these values are decreased by extending the stages of VM cells [18, 19, 23, and 26]. Since the active switches of the suggested structure are clamped to VM units' capacitors, the normalized peak voltage amongst the power switches is limited to a lower value by enhancing the number of VM cells. Additionally, utilizing a lower conducting resistance power switch, leads to limit of the power components loss of the converter. The overall cost of the structure can be alleviated by applying a lower rating power MOSFET.

Fig. 5(c) indicates the maximum voltage rates upon diodes against voltage gain (normalized voltage stress amongst diodes versus voltage gain). The voltage stress over the power diodes is limited to a lower value when the voltage gains increases, considering the presented curves of Fig. 5(c). The power rating of the presented topologies is enhancable by developing the number of VM stages, and this circumstances the normalized maximum voltage throughout the active semiconductors (MOSFET/diode) have lower amounts [22, 24, 25]. Therefore, using a lower power ranges diode leads to increase in the system overall efficiency and leads to a cost effective converter, the recommended structure presents lower loss for all power limits.

Table 1 shows the advantages and disadvantages of the presented topology and other topologies. Generally, to highlight the advantages of the presented circuit to the other structures, some comparison is included in Table 1.

Table 1 The presented topology comparison with other topologies.

Converter	M_{CCM}	M_S	M_D	NO. of switch	NO. of diode	NO. of capacitor	NO. of inductor	Input current ripple (%)	Efficiency [%]
Proposed	$\frac{5+2n-D}{1-D}$	$\frac{M_{CCM}-1}{(4+2n)M_{CCM}-10-4n}$	$\frac{M_{CCM}-1}{(4+2n)M_{CCM}-10-4n}$	4	2(n+2)	2n+5	4	4	94.6 [350W]
[18]	$\frac{2+N(3-D)}{1-D}$	$\frac{M_{CCM}-N}{2(N+1)M_{CCM}+2(N-1)}$	$\frac{N(M_{CCM}-N)}{2(N+1)M_{CCM}+2(N-1)}$ $\frac{(N+1)(M_{CCM}-N)}{2(N+1)M_{CCM}+2(N-1)}$	1	5	5	1	48	91.3 [350W]
[19]	$\frac{3+2N}{1-D}$	$\frac{3}{3+2N}$	$\frac{3}{3+2N}$	3	4	4	3	18	94.1 [350W]
[20]	$\frac{N+2}{1-D}$	$\frac{1}{N+2}$	$\frac{N+1}{N+2}$	1	3	3	1	100	92.2 [350W]
[21]	$\frac{4}{1-D}$	0.25	0.5	2	5	5	2	10	90.2 [350W]
[22]	$\frac{4+2N}{1-D}$	$\frac{1}{4+2N}$	$\frac{1}{2+N}$, $\frac{1+N}{2+N}$	2	*4*	*4*	2	54	93.3 [350W]
[23]	$\frac{6}{1-D}$	1/3	1/3, 1/6	1	7	6	3	24	93.2 [350W]
[24]	$\frac{(1+N)(1+D)}{1-D}$	$\frac{M_{CCM}+N+1}{2M_{CCM}(N+1)}$	$\frac{M_{CCM}+N+1}{2M_{CCM}(N+1)}$	1	4	5	2	20	94.3 [350W]
[25]	$\frac{3+2N-D(1+N)}{1-D}$	$\frac{M_{CCM}-N-1}{M_{CCM}(N+2)}$	$\frac{M_{CCM}-N-1}{M_{CCM}(N+2)}$	1	4	4	1	38	92.1 [350W]
[26]	$\frac{n(1-D)+2-D}{1-D}$	$\frac{M_{CCM}-n-1}{3M_{CCM}}$	$\frac{M_{CCM}-n-1}{3M_{CCM}}$	1	n+3	2n+3	n+1	100	94.3 [350W]
N*, *n	n= VM unit		N= turns ratio (N is considered 2)						

The normalized peak voltage on the switches and diodes of the converter has lower values and this value is decreased by increment in the power level (by extending the number of VM units). The suggested converter capable to transfer a high power level by adding the stage of VM units. The most outstanding advantages of the presented converter are utilizing lower rating power semiconductors, capable to transfer a high power rate with higher efficiency and limited overall cost.

5 Experimental

In this part, an experimental prototype of the recommended converter with n=1,2 stage in CCM operation is manufactured and tested, besides the laboratory results of the presented structure are prepared in Figs. 6-10 to prove the correctness of theoretical survey. The *ATmega* 16 is used to generate gate signals of the power MOSFETs with 40 kHz switching frequency. All used elements are provided in Table 2 and also a ceramic resistors with various ranges are used as a load.

Table 2 demonstrates the components configuration of the suggested structure. Table 3 illustrates the comparison of the technical, simulation and laboratory results of the suggested structure, which these values are confirmed each other.

Table 2 Components used in the converter

Parameter	Value
Input voltage	24 *V*
Switching frequency	40 *kHz*
Duty cycle	0.6
R	430Ω for n=1 500Ω for n=1
Inductors L_1 , L_3	480 μH
Inductors L_2, L_4	1 *mH*
Capacitors of VM units	330 μF
C_{o1}, C_{o2}	330 μF
C_o	470 μF
Power MOSFETs	IRFP260
Power diodes	MUR1560

Table 3 Theoretical, simulation and laboratory results of the recommended topology

Parameter	k=1			k=2		
	Mat.	Sim.	Exp.	Mat.	Sim.	Exp.
$V_{S1\text{-}peak}$ [V]	60	59.3	59.4	60	59.2	59.3
$V_{S2\text{-}peak}$ [V]	84	82.9	83.1	84	82.6	82.8
$V_{D11\text{-}peak}$ [V]	60	59.3	59.4	60	59.1	59.1
$V_{Do1\text{-}peak}$ [V]	84	82.6	82.9	84	82.4	82.6

Fig. 6 demonstrates the measured efficiency of the suggested topology based on the power rating and load current at the CCM operation. With regarding Fig. 6 (a), the maximum efficiency of the suggested structure is achieved about 95.83% which

the power value is about 70W at this point. Generally, the minimum efficiency of the recommended topology is almost 91.2% in all power levels. Generally, the efficiency of the presented structure has a little tolerance (about 4.63%) at all power ratings. Also, the performance of the recommended topology is large at higher power levels when the number of VM units is increased. The maximum efficiency point has happened in higher power ranges for the larger number of VM units at a higher power value rather than the lower number of VM units. Fig. 6(b) demonstrates the efficiency of the suggested converter based on current load change.

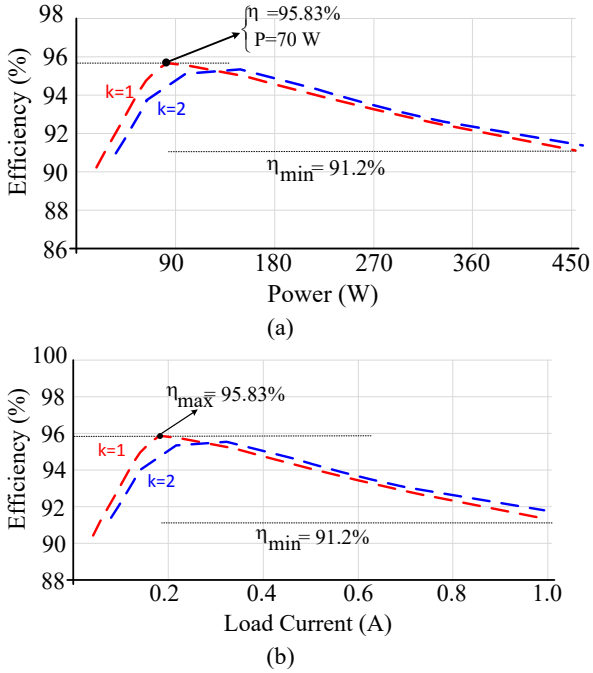


Fig. 6 The measured efficiency (a) Versus power level for k=1, 2, (b) versus load current for k=1, 2.

The maximum performance rate of the suggested converter is obtained approximately 0.18A and the minimum efficiency is limited to 91.2% by increasing current load. Figs. 7-10 show the laboratory results of the presented converter with k=1, 2 stages in CCM operation which Figs. 7 and 8 are related to k=1 and Figs. 9 and 10 are related to k=2. Fig. 7(a) indicates the capacitor C_{11} voltage for k=1. This value is obtained by about 59.3V which is confirmed (35). The voltage value of the capacitors C_{o1} and C_o are shown in Fig. 7(b) which the obtained value is equal to about 195V and 389V, respectively. Also, the obtained equations in (39) and (41) confirms these results. Fig. 7(c) indicates the inductors L_1 and L_2 current waveforms. It is observed by the figure that the inductor L_1 current ripple content is from 1.92A until 2.72A, and the inductor L_2 current rate fluctuates between 5.35A and 5.75A. Therefore, the percent current fluctuation of the inductors L_1 and L_2 is about 35.3% and 7.2%, respectively. Fig. 7(d) shows the current waveforms of the inductors L_3 and L_4. Regarding Fig. 7(d), the current ripple of the inductors L_1 and L_3 equivalent to each other, L_2 and L_4 equal each other, just have a phase shift each other. The percent current ripple of the inductors L_3 is equal to about 33.5% (from 1.93A until 2.70A) and the percent current ripple of the inductor L_4 is identical to about 7.7% (from 5.33A until 5.76A).

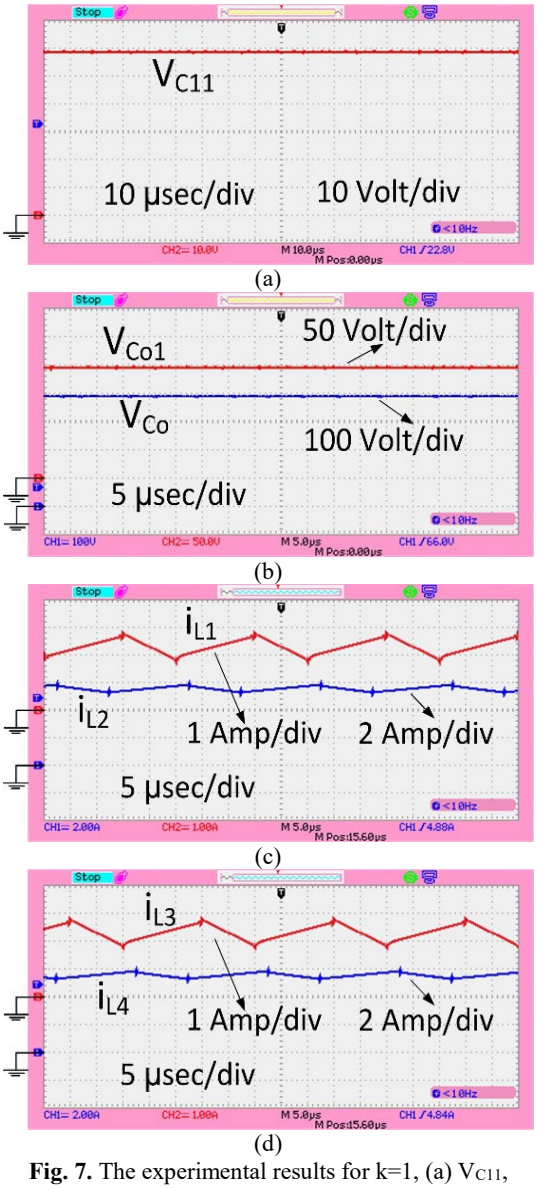


Fig. 7. The experimental results for k=1, (a) V_{C11}, (b) V_{Co1} and V_{Co}, (c) I_{L1} and I_{L2}, (d) I_{L3} and I_{L4}.

Fig. 8 exhibits the peak voltage of the semiconductors devices (MOSFETs/diodes). Fig. 8(a) represents the utmost voltage value of the switches S_1 and S_2, in which these values are obtained 59.4V and 83.1V, respectively. Fig. 8(b)

indicates the uppermost voltage of the active switches S_3 and S_4, in which these values are obtained about 59.3V and 83.2V, respectively. Fig. 8(c) demonstrates the peak voltage content of the active diode D_{11}. This value is obtained 59.4V which confirms (43). Fig. 8(d) indicates the peak voltage content of the power diode D_{o1} (82.9V) that confirms (46).

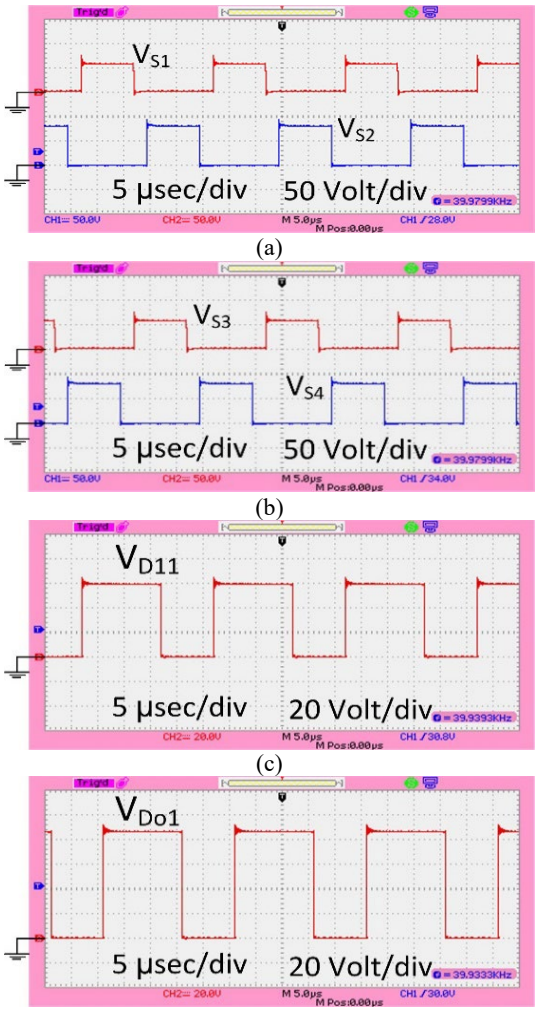


Fig. 8 The maximum voltage of the semiconductors with k=1, (a) V_{S1} and V_{S2}, (b) V_{S3} and V_{S4}, (c) V_{D11}, (d) V_{Do1}.

Fig. 9(a) demonstrates the voltage of the capacitor C_{11} for k=2 which is equal to about 59.2V which is confirmed (35). Fig. 9(b) depicts the voltage of the capacitor C_{o1} and output capacitor C_o. The capacitors C_{o1} and C_o voltages value are equal to about 252V and 479V, respectively. Fig. 9(c) proofs the inductors L_1 and L_2 current waveforms which the percent current ripple of these inductors are about 31.8% (from 1.85A until 2.55A) and 4.6% (from 8.45A until 8.85A), respectively. Fig. 9(d) represents the current waveform of the inductors L_3 and L_4. Besides, the current ripple contents of the inductors L_3 and L_4 is about 30.9% (from 1.86A until 2.54A) and 5.1% (from 8.43A until 8.87A), respectively.

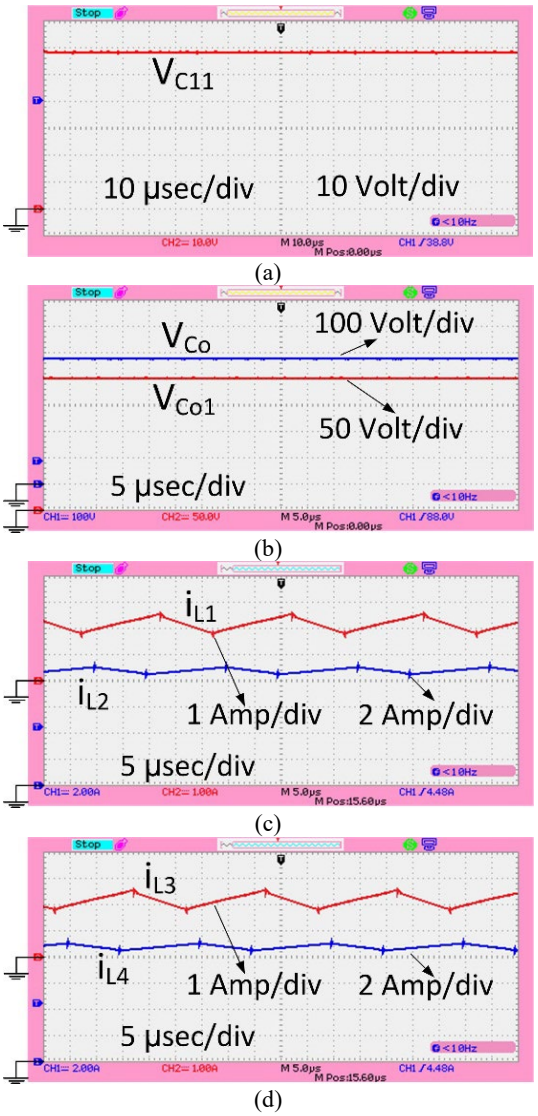
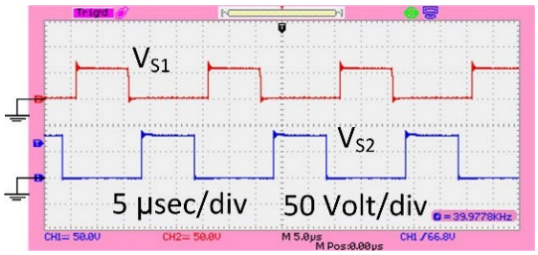


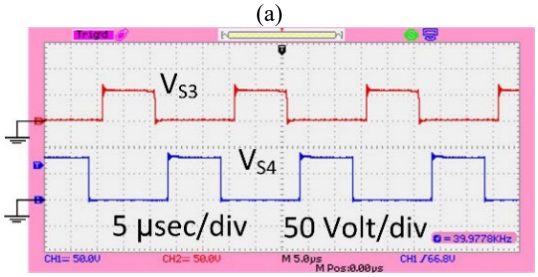
Fig. 9 The experimental results for k=2, (a) V_{C11}, (b) V_{Co1} and V_{Co}, (c) I_{L1} and I_{L2}, (d) I_{L3} and I_{L4}.

Fig. 10 describes the maximum voltage of the switches S1 and S2. The obtained value of these switches is 59.2V and 82.6V, respectively. Fig. 10(b) indicates the maximum voltage, per the switches S3 and S4 which are about equal to the maximum voltage content of the active switches S1 and S2, respectively. Figs. 10(c) and (d) show the peak voltage values of the active diodes D11 and Do1, which are equal to 59.1V and 82.6V, respectively. Fig. 11 illustrates the laboratory prototype of the proposed converter. Generally, based on obtained experimental waveforms, it can be said that the suggested converter has a remarkable voltage gain. The voltage gain is more increased by extending the VM stage number. Also, it has been

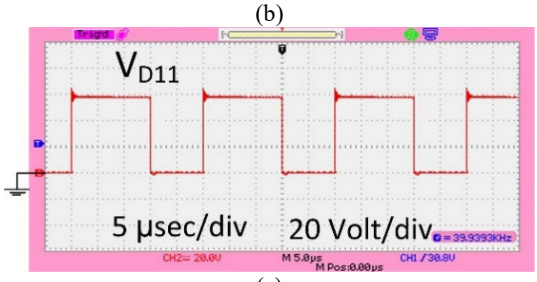
clarified that the normalized upmost value of voltage amongst the active semiconductors is low and subsequently decreased by extending the stages. Besides, the current ripple of the inductors is decreased by increasing VM stages (in fact for high power levels). Therefore, the power components with lower ratings are used in the proposed converter. However, it cannot be denied that the number of power components is enhanced by adding the VM stages. Generally, the overall efficiency of the recommended structure is high and the normalized peak voltage throughout the semiconductors (MOSFETs/diodes) is diminished by increasing the power level. Since the power losses of power semiconductors have an important role in overall cost and industrial applications, it is derivable that the presented structure is a proper choice for renewable systems.



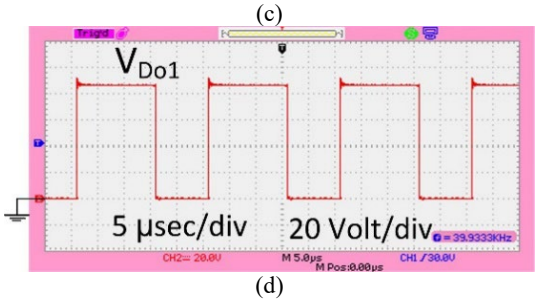
(a)



(b)



(c)



(d)

Fig. 10 The maximum voltage of the semiconductors with k=2, (a) V_{S1} and V_{S2}, (b) V_{S3} and V_{S4}, (c) V_{D11}, (d) V_{Do1}.

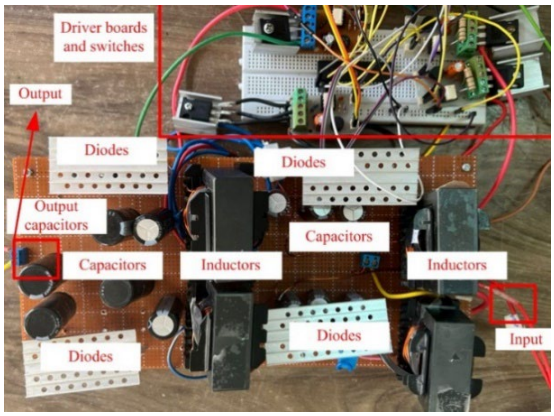


Fig. 11 The laboratory prototype of the proposed converter.

6 Conclusions

A new dc-dc converter with a higher voltage converting rate employing VM is suggested. The voltage gain of the converter increases via cascading VM stages to each other. The normalized maximum voltage above the semiconductors is decreased by adding the number of VM units. Generally, the number of power components in the presented structure is enhanced by adding VM stages, where the converter cost can be decreased by utilizing the lower rated semiconductors (MOSFET/diode). The overall efficiency of the suggested converter is higher than 91.2% in all load powers. The maximum performance rate of the presented structure is about 95.83%. Generally, the proposed converter can be could be appropriate for sustainable applications based on lower input current ripple using interleaved techniques, lower losses on semiconductors, high voltage conversion ratio and high load power rating. The laboratory results of the presented topology with n=1, 2 for 350W and 453W in operating frequency at 40 kHz are tested and the achieved results of the experimental results are confirmed as well as the theoretical analysis. As a result, by considering these circumstances, it is noticeable that the recommended could be proper choice for green source applications like PV generation, fuel cells, etc.

Intellectual Property

The authors confirm that they have given due consideration to the protection of intellectual property associated with this work and that there are no impediments to publication, including the timing to publication, with respect to intellectual property.

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CRediT Authorship Contribution Statement

A. Gallaj: Idea & Conceptualization, Research & Investigation, Data Curation, Analysis, Methodology, Project Administration, Software and Simulation. **J. Fallah-Ardashir:** Supervision, Verification, Original Draft Preparation, Revise & Editing, Methodology, Project Administration. **M. Beiraghi:** Supervision, Verification, Original Draft Preparation, Revise & Editing.

Declaration of Competing Interest

The authors hereby confirm that the submitted manuscript is an original work and has not been published so far, is not under consideration for publication by any other journal and will not be submitted to any other journal until the decision will be made by this journal. All authors have approved the manuscript and agree with its submission to "Iranian Journal of Electrical and Electronic Engineering".

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