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Research Paper

Ultra-Low Power 5T-SRAM Cell Design using different CNTFET for exploiting Read/Write Assist Techniques

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Abstract: In today's technological environment, designing the Static Random Access Memory (SRAM) is most vital and critical memory devices. In this manuscript, two kinds of 5TSRAM are designed using different CNTFET such as Dual-ChiralityGate all around (GAA) CNTFET and Ballistic wrap gate CNTFET based 5T SRAM cell designs for enhancing the read/write assist process. Here, the proposed Dual-ChiralityGAA-CNTFET based 5T-SRAM has two cross-coupled inverters using one access transistor that is connected to the bit line (BL) and word line (WL) through minimum supply voltage. Instead of cross-coupled inverter circuit, the BWG-CNTFET based 5T-SRAM cell is intended for achieving less power and improved read/write assist process. Also, one transistor is executed as low-threshold (LVT) device in the proposed BWG-CNTFET based 5T-SRAM. Thus, proposed two kinds of 5T SRAM cells increases the read/write assist operation and reduce the leakage current/ power. The simulation of the proposed two kinds of 5T SRAM cell is done by HSPICE simulation tool and the performance metrics are calculated. Therefore, the proposed Dual-ChiralityGAA-CNTFET based 5T-SRAM cell design has attained 11.31%, 51.47% lower read delay, 44.44%, 26.33% lower write delay, 36.12%, 45.28% lower read power, 34.5% , 22.41% lower write power, 37.4%, 15.3% higher read SNM and 35.8%, 12.09% higher write SNM than Double gate carbon nanotube field effect transistors (DG CNTFET) and state-of-art method respectively. Similarly, the proposed BWG-CNTFET 5T SRAM cell design has attained 45.53%, 38.77% lower write delay, 56.67%, 45.64% lower read delay, 58.4%, 56.75% lower read power, 49.66%, 28.56% lower write power, 35.32%, 12.7% higher read SNM and 45.8%, 15.6% higher write SNM than Reduced Power with Enhanced Speed (RPES) approach and state-of-art method respectively.

Keywords: Ballistic Wrap Gate, Carbon Nanotube, Dual-Chirality, Field Effect Transistor, Static Random Access Memory, read/Write Assist Method

1 Introduction

RECENTLY, the integrated circuit with high performance is executed in deep submicron technology [1, 2].

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Numerous works are performed under design and enlargement of convenient devices to develop the applications includes entrenched medical equipment's, space applications and wireless body sensing networks [3, 4]. These applications require the design of lower power semiconductor memory devices [5]. A substantial part of a system-on-chip area is covered by conventional 6T SRAM (Conv.6T SRAM) [6, 7]. As technology shrinks, power intemperance becomes a prominent factor damaging backup battery for manageable device [8]. Decreasing in supply voltage is a general approach that decreases power dissipation from the SRAM cell [9, 10]. To improve performance and increase stability in areas such as balance, various

researchers have presented numerous SRAM cell topologies, like 7T, 8T, 9T, 10T [11, 12]. Transistor count is decreased to compensate for area and also preserves greater performance [13-16]. The scale down at the technology node, concern maximizes static power dissipation [17].

For diminishing leakage power dissipation, several power approaches are suggested, such as leakage feedback, stacked driver, body bias, and sleepy driver approach [18]. On the other hand, the data is not retained on the storage nodes. This problem is eradicated through the self-controlling voltage level switch circuit that maintains performance and decreases static power dissipation [19]. The sub-threshold SRAM cell is imaginable selection that decreases stand-in power circuit [20]. Conversely, the main constraint related to the sub-threshold section has low read stability/delicate the write ability [21]. In addition, the SRAM based on schmitt-trigger cell introduced the write ability and read strength concurrently for improvement. In this cell, the three-door structure uses a smaller area and admits less static power by enhancing the static noise margin (SNM) [22]. The access time to the SRAM cell is corrupted to reduce gate current under sub-threshold operation. This problem is eradicated to reduce the floodgates at each phase of the pipeline [23].One more limitation of sub-threshold region is small value of ratio destroys the noise margin cell [24]. However, the existing SRAM Cell designs are attained some limitations in read and write operations, which are utilized high power and delay [25-31]. Thus, to overcome those issues, CNTFET based 5T SRAM cell designs are proposed in this manuscript.

Main attributes of this work is given in detail,

- In this research work, low power 5T SRAM Cell designs using CNTFETs is proposed to improve read/write assist performance.
- Here, the Dual-Chirality Gate all around (GAA) CNTFET based self-controlled 5T SRAM cell design [23] and Ballistic wrap gate CNTFET based 5T SRAM cell design [24] with self-controllable voltage level (SVL) circuit.
- Thus, the proposed Dual-Chirality GAA-CNTFET and BWG-CNTFET based self-controlled 5T SRAM methods are utilized increases read/write assist operations and reduces the leakage current/ power.
- Finally, the performance of the proposed CNTFET 5T SRAM cell design is scaled based on area, read delay, read power, write delay, read speed, write power, write speed, power delay product (PDP), stability analysis using Static Noise Margin (SNM).
- The implementation of proposed model is implemented on HSPICE simulation tool and the performance of proposed model is likened to conventional SRAM.
- The performance analyses of proposed DC-GAA-5CNTFET-SRAM cell for read/write (R/W) assist process related to DG CNTFET [25] and state-of-art method respectively.
- Similarly, the performance of proposed BWG-5CNTFET-SRAM for R/W assist process is related to existing approaches, like Reduced Power with Enhanced Speed (RPES) approach [27], and state-of-art method respectively.

Rest of the manuscript is organized below as: section 2 reviews that Literature survey, section 3 describes proposed Dual-Chirality GAA-CNTFET based self-controlled 5T SRAM design. Also, Section 4 detailed about the BWG-CNTFET based self-controlled 5T SRAM design. Section 5 detailed results and discussion. At last, Segment 5 completes the manuscript.

2 Related Works

Ponnayan et al., [25] have presented an instruction set computer through optimized polarity tunable model of DG CNTFET. Here, the dielectric constant and gate oxide thickness are enhanced to overwhelm ambi polar conduction on CNFETs. To optimize these parameters, an approach based on multi-objective genetic algorithms was suggested. Initially, a double gate carbon nanotube FET with improved parameters was devised. By manipulating the capacitance that chooses transmission behavior by means of a second gate in double-gate carbon nanotube FET, the device is electrostatically programmed to realize carbon nanotube FET n-type/p-type. Second, a computer with an instruction set replicated the optimized model of double-gate carbon nanotube FET. The presented approach provides better performance based on the condensed count of logical levels. Conversely, the suggested approach provides higher read delay.

Jooq et al., [26] have introduced robust and minimum-power near-threshold SRAM cell using ballistic carbon nanotube wrap-around gate transistors. The presented SRAM cell has been specifically intended to mitigate the demand to use complex bit training circuits for reloading bit lines through operations. The higher threshold voltage

multi-tube carbon nanotube field-effect transistors biased under near-threshold region to attain reasonable data transfer rate and power efficient operation. The presented approach has the potential for a large memory array, but requires high power consumption.

Alekhya and Nanda [27] have presented fast and power efficient SRAM cells based on CNTFETs for edge AI devices. In this, a reduced power enhanced speed (RPES) approach to SRAM using CNTFETs, smart portable devices and high speed. Each SRAM cell was examined for numerous maximum-k dielectric materials, and pitch values of CNFETs and the best fit outcomes presented in SRAM. The presented approach reduces the propagation delay but the leakage of current using the suggested approach is high.

Elangovan et al., [28] have introduced maximum stable and minimum power 8T Carbon Nano Tube Field Effect Transistors SRAM cell. The performance of 8T SRAM cells presented for nominal and dual chiral value is likened to conventional 6T and 8T cells. The simulation was performed by using Stanford University 32 nm CNFETs model on HSPICE simulation tool. The presented approach consumes less power but it takes higher delay in read/write operations.

Elangovan et al., [29] have introduced darling Ton-based 8T CNFETs, SRAM cells using less power and improved write stability. In this case, a Darlington-based 8T SRAM cell with lower power and increasing write margin was suggested. The power consumption of presented Darlington static random access memory cell was compared to other static random access memory cells. The suggested SRAM Darlington cells power consumption is lower compared to conventional 6T and 8T CNTFET SRAM cells for write, hold and read operations. The write static noise margin (WSNM) of the presented approach is found to be higher alternatively, it takes high power consumption.

Shrivastava et al., [30] have presented the compact design, reliable and energy efficient CNFET 17T ternary S-RAM cell. In this ternary SRAM cell with no read disturbances with 17 CNFETs. The presented ternary SRAM cell operates two voltage levels and stores three levels of high, low and medium voltage. The presented SRAM was energy efficient since the power delay product (PDP) was low. The featured memory cell suffered from temperature and process mismatches. The featured ternary memory cell was less exaggerated by process and temperature differences. The presented ternary SRAM cell was shown to be robust against carbon nanotubes and CNFET channel length variation on Monte-Carlo analysis. In this, the presented approach acquires minimum area and it takes maximum time.

Srinivasu et al., [31] have presented less power and higher performance ternary SRAM design using the application of CNFETs technology. In this, presented a two efficient ternary SRAM design was applicable to various technologies based on transistor. The initial design depending on loop operator under ternary logic, although the second was buffer-based design works with positive as well as negative. In cooperation with the design, it consumes less power compared to existing standard ternary inverter fed static random access memory designs. The presented designs also have noise margin comparable design. In this, the presented approach shows lower read and write delay. But power consumption is higher.

3 Proposed Self-controlled CNTFET Based 5T-SRAM Methodology

In this work, Dual-Chirality (DC) Gate all around (GAA) CNTFET and Ballistic wrap gate CNTFET based self-controlled 5T-SRAM cell designs are proposed to improve the read/write assist process and to attain low power. Initially, the DC-GAA-CNTFET based 5T-SRAM cell is designed that has two cross-coupled inverters , one access transistor linked to bit line (BL) and word line (WL) through minimal supply voltage. Additionally, the BWG-CNTFET based 5T-SRAM cell is designed low-threshold (LVT) device and right BL is held less through the standby operation as well as read operation. Therefore, the proposed 5T SRAM cell designs are enhancing R/W assist process and reduced the leakage current/power.

3.1 Basic Theory

SRAM is the basic component of the CPU in a computer. In the IC, all the contents of dissimilar circuits are combined into a single chip. With the presentation of the IC, the microprocessor (MP) and the entire devices are placed at monolithic device named microcontroller. In the microcontroller, all the essential components are built together. The microcontroller also stores data through the use of SRAM. The microcontroller consists of registers, RAM, Memory, and circuitry for control. SRAM is a kind of RAM in which the word static means that the date that is stored can be retained insufficiently, without the need for a periodic refresh operation as long as appropriate voltage is supplied. SRAM is quicker to DRAM

because their commercial chips accept the entire address bits at once. Two strong ways are utilized to save leakage and active current. Firstly, the reduction of the operating voltage, and secondly, the reduction of the capacitance of the BL and WL. According to survey, it is found that up to 70% power is consumed based on discharge or charge of the bit lines through the R/W modes. To validate the design, the write static noise margin (WSNM) is derived to predict the noise margin values. This model is required for general WSNM estimation and eliminate extensive simulation for low-tech nodes, which will reduce CPU time. The proposed analytical model deals with the physics of the device and aids to relate the analytical outcomes with the simulation outcomes. The following two probable cases contemplates under the present case for WSNM.

The standard SRAM 5T is made up of two cross-coupled inverters (INV-1 and INV-2) and access transistors (MA1), which connect the cell to the bit lines (BL). The cross-coupled inverter pair is made up of load transistors (MP1 and MP2) and control transistors (MN1 and MN2) that are stronger to access transistors. If BL is set high and the WL is asserted, the transistors MA1 and MN1 fight each other. To ensure a successful write operation happen, it is significant to consider storage node It must increase (or fall) above (or below) the trigger voltage of INV-2 in the WL is logic high, otherwise the write error will happen. In more detail, when writing a logic '1' to a cell while initially storing a logic '0', the cell's low storage node A should be pulled up through the pre-loaded BL above the trigger voltage of INV-2.

To solve '1' write problem of traditional SRAM 5T cells, numerous methods have been established. Some of these methods based on increased WL voltage, VDD supply voltage stepping down, cell transistor sizing, bit stepping down line voltage, and VSS source voltage stepping up. Nevertheless, every methods cause a reduction on transistor drive current and cell operating speed, or increase memory cell area and a degradation in manufacturing accuracy, or need the generation of a voltage, or it needs the more complicated circuit design. Therefore, it is a require for an effective methods to enhance write-ability of SRAM 5T cells that cannot write '1'.Thus, in this work, transistors are replaced with CNTFET. Initially, the Dual-Chirality GAA-CNTFET SRAM model is designed and the stability of read and write assist processes are analyzed. Moreover, Ballistic wrap gate CNTFET SRAM model is designed and the stability of read and write assist processes are analyzed. Finally, the efficacy of the proposed two designs are analyzed by various performance metrics like power, delay, and area. The designing method of proposed DC-GAA-CNTFET and BWG-CNTFET based 5T-SRAM cells are detailed as below. Figure 1 shows the Circuit diagram of the 5T SRAM cell design.

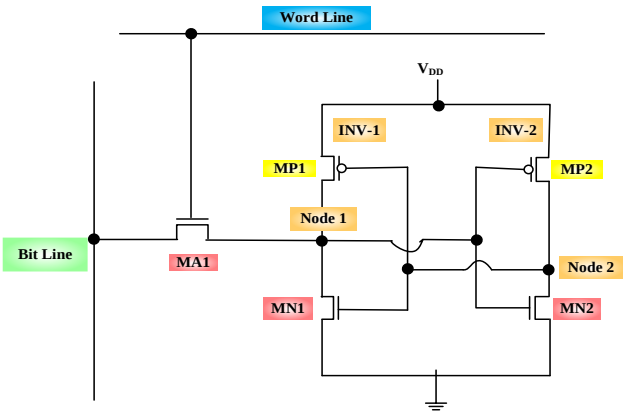

Fig. 1 Circuit diagram of the 5T SRAM cell design.

3.2 Design of Dual-Chirality GAA CNTFET Self-controlled 5T SRAM Cell

In this work, the Dual-Chirality GAA-CNTFET based 5T-SRAM cell design is proposed for less power and maximum Read/Write Assist performance. In proposed DC-GAA-CNTFET, the threshold voltage is adjusted through chirality vector controlling. In this work, different diameters or chirality are utilized for GAA-CNTFET based self-controlled 5T SRAM that are N-type and P-type. Here, self-controlled SRAM is an important reducing power delay product and improving SRAM stability. Moreover, the proposed Dual-Chirality GAA-CNTFET based 5T-SRAM has two cross-coupled inverters through one access transistors that linked to BL, WL through minimal supply voltage. Subsequently, the performance of the proposed Dual-Chirality GAACNTFET fed self-controlled 5T SRAM cell design are measured based on delay, leakage power, power delay product (PDP), stability analysis based Static Noise Margin (SNM). Additionally, block diagram of Dual-Chirality GAA CNTFET self-controlled 5T SRAM cell is shown in Fig. 2.

The optimal chirality is designated for achieving best performance related to its stability, power consumption, write time of GAA CNTFET 5T SRAM cell. Additionally, threshold voltage of CNTFET depends on chirality vector of GAA CNTFET. Hence, GAA CNTFETs provides unique opportunity to control threshold voltage through the changing diameter of CNTFET. The N-type GAA CNTFETs and P-type GAA CNTFETs uses CNTs, this has various chirality vectors for better performance. Conversely, N-type GAA CNTFETs and P-type GAA

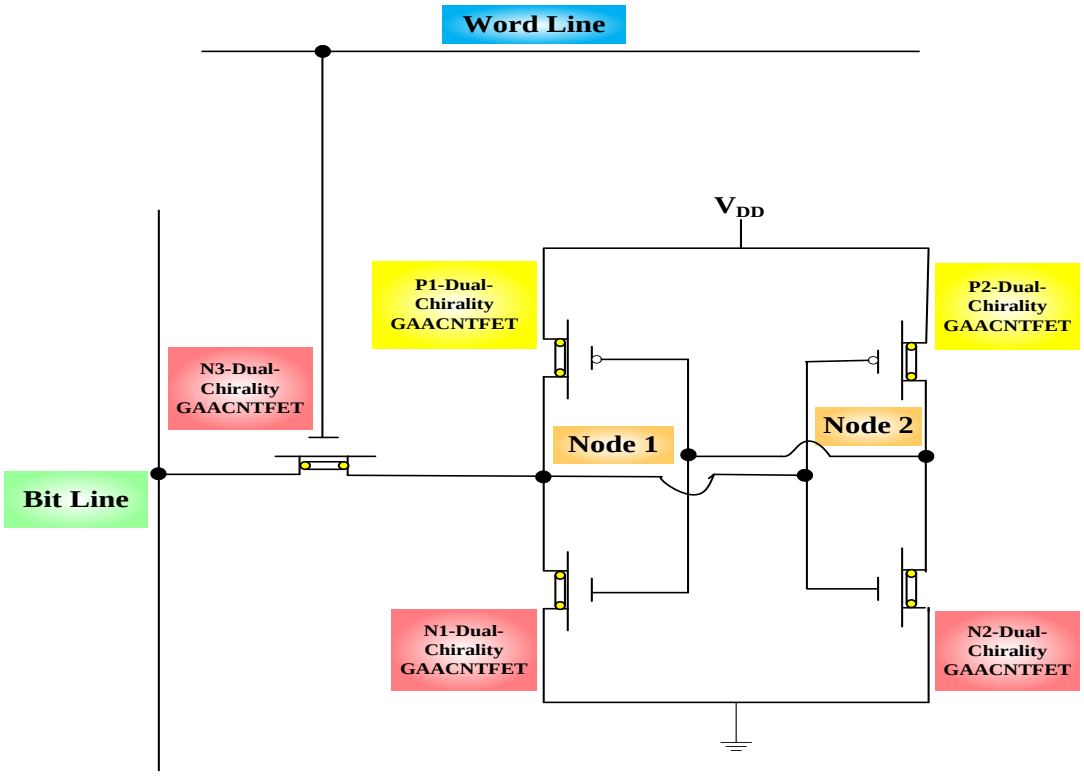

Fig. 2 Block diagram of dual-Chirality GAA-CNTFET based 5T-SRAM.

CNTFETs uses similar chirality vector CNTs. Moreover, novel index for dual-chirality GAA CNFETs-based SRAM design is mentioned as (*cp*, *cn*, *cv*), where, first chirality vector is mentioned as *cp*, *cn* of P-type GAA CNTFETs and N-type GAA CNTFETs refers common 2nd chirality vector consist of 2 kinds of GAA Carbon Nano Tube Field Effect Transistors that is mentioned a *cv*.

Typically, 5T-SRAM cell using R/W assist technique consists of integrated memory arrays. SRAM memory matrix has rows and columns that are located as point of WL and BL. Also, it is gathered into smaller rows of greater columns in which SRAM array rows are utilized for WL and SRAM array columns utilized for BL. Row decoder utilizes the address for activating one of the rows through declaring the word line. Similarly, the column circuitry utilizes the address for activating one of the columns through declaring the BL. If WL is represented at V_{DD}, then time writing 1 or 0 is performed on Dual-Chirality GAA CNTFETs based 5T-SRAM cell delivered with BL voltage as 1.85V to V_{DD} and 0V to V_{SS}.

If logic great (V_{DD}) is used at cross coupled inverter from input, the P-type DC-GAA-CNTFET does not operate and N-type DC-GAA-CNTFET operate. Likewise, if logic low (V_{DD}) is used at cross coupled inverter from input, then P-type Dual-Chirality GAA CNTFET will work and N-type Dual-Chirality GAA-CNTFET will not operate.

In this design, access transistor denoting the pass transistor, which is utilized for assisting techniques such as R/W operation. Additionally, writing operation of proposed model has a condition that is given in Eq. (1):

$$V_{DD} = V_{BL} = V_{WL} \tag{1}$$

where, V_{DD} denotes supply voltage, V_{BL} represent BL voltage, and V_{WL} represent WL voltage. Additionally, reading operation happened in the proposed model has condition that is given in Eq. (2):

$$V_{SS} < V_{dual\_C} < V_{DD} \tag{2}$$

Where, V_{SS} denotes the ground voltage in the design, and V_{dual_C} denotes the voltage in dual-chirality. Subsequently, the working procedure of the design is based on three operations that are hold, read, and write, which are detailed as below:

- **Hold operation**

The word line is equal to zero for detent operation, in which the operation of the dual-chirality CNTFET GAA-based self-controlled 5T SRAM acts as the cross-coupling latch storing the data from 1 and 0. No flow current on circuit during word line is zero, since the access transistor is not turned on. Subsequently,

the access transistor (AT) implies N-type Dual-Chirality GAA CNTFET *N3* that is not stimulated when WL is zero. Therefore, the BL is disconnected as cross-coupled latch operation.

- **Read operation**

In this operation, at first make bit line to dual-chirality and retain the WL denotes low. Also, output is obtained from BL. Moreover, voltage value of *N3* dual-chirality is mentioned as V_{dual_C}=625mV to V_{dual_C}=675mV using external supply voltage that is utilized for BL. Subsequently, BL set as V_{dual_C} that can set the word line as 1. At that time, the current flow is produced on circuit since the access transistor is stimulated when the WL implies zero. Thus, access transistor of the proposed N-type dual-chirality GAA CNTFET *N3* is activated, when WL is equal to one. Additionally, the BL is utilized for increasing speed of operation to latch circuit.

Figure 3 shows that read operation of proposed DC-GAA-CNTFET at Reading='0' condition. Let the reading operation as zero, and then the bit line is pulled down by N-type DC-GAA-CNTFET transistor, which is combined form of *N1* dual-chirality and *N3* dual-chirality. Additionally, the main reason of pull down BL refers voltage variation among BL and the value of node refers zero, which can diminish the BL voltage. Subsequently, the BL voltage is retained when the node value is one that is occurred when it is no voltage variation. After that, the BL values are given to the sense amplifier of proposed model.

Additionally, the sense amplifier of proposed model acts as operational comparator circuit that can compare the BL values of node A and B, which provides the output. There are two kinds of condition in the sense amplifier for producing the outputs that are i) $BL(node\_A) > BL(node\_B) = 1$ that means if the value of node A bit line is greater than node B bit line then the condition is 1, ii) $BL(node\_A) < BL(node\_B) = 0$ that means if the value of node A bit line is less than node B bit line then the condition is 0.

Figure 4 depicts the read operation of proposed dual-chirality GAA-CNTFET at Reading='1' condition. In this condition, the current is passed through the circuit when the word line is equal to one. In this stage, the access transistor refers N-type DC-GAA-CNTFET *N3* activated when the WL is equal to one, which can connect the storage node with BL to latch circuit. Subsequently, consider the reading operation is 1 then the BL is pulled up by P-type dual-chirality GAA-CNTFET transistor *P1*. Thus, the BL voltage will get engaged. Also, the BL voltage get reduced by node B=0 since there is a voltage variance among BL and node B. Therefore, the BL of node A and B are provided with sense amplifier. Subsequently, if BL value of node A is greater to BL values of node B, then sense amplifier produce the output as 1. If A=1, the data read through sense amplifier is also 1, so it properly reads data from 1.

- **Write operation**

In write operation, WL is set as one, and then current flow is produced on circuit since the access transistor of the proposed N-type DC-GAA-CNTFET *N3* is activated when the word line is one. This function can also connect the storage node as BL to latch circuit. Subsequently, bit line of model is act as the input on write operation.

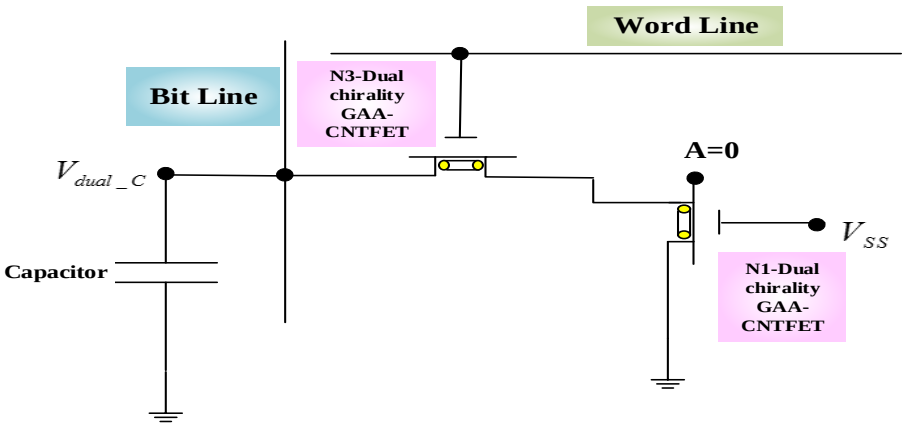

Fig. 3 Read operation of proposed dual-chirality GAA CNTFET (Reading='0').

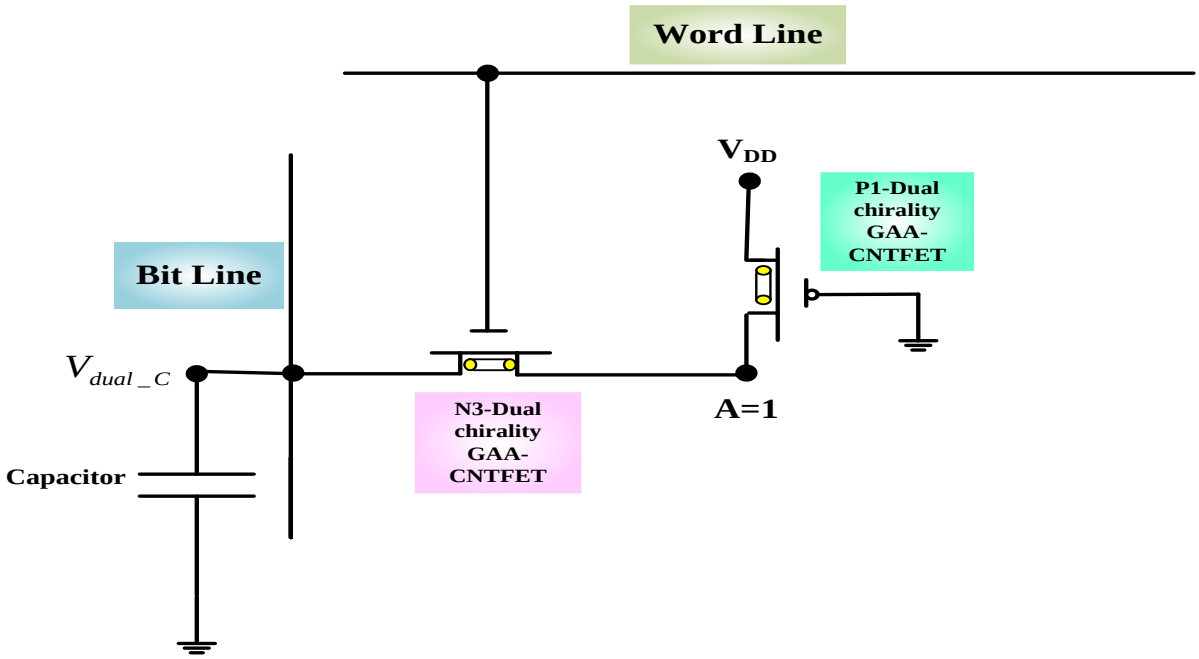

Fig. 4 Read operation of proposed DC-GAA-CNTFET (Reading=’1’).

3.2.1 Stability Analysis

It is one of the main factors used to design SRAM. For designing, the SNM metric is used for the purpose of stability. Normally, the SNM is an amount of stability for the SRAM cell that holds their data against noise. SRAM's SNM is constrained in that less amount of noise voltage is essential at SRAM's storage terminals to change the state of cell. Detailed discussion on stability analysis is given below.

- **Hold Stability**

It is necessary concern while maintaining the '0' state of proposed DC-GAA-CNTFET-5T-SRAM, wherever the deficiency of positive feedback to flip the cell so that the selection of appropriately sized transistor through threshold implants provide the necessary stability. Additionally, hold '1' level is governed by leakage current rates, and increasing at low voltage can trigger destructive positive feedback.

- **Read Stability**

In dual-chiralityGAA-CNTFET-5T-SRAM, read stability is the necessary metric since it accidently writes based on read the stored value. Also, the P-type voltage DC-GAA-CNTFET *P1* transistor and N-type DC-GAA-CNTFET transistor *N1*, *N3* surpasses switching voltage of P-type dual-chirality GAA-CNTFET *P2* transistor as well as N-type DC-GAA-CNTFET *N2* through reading stored “0” operation. If channel length modulation is disregarded, and then the current passed through access transistor N-type DC-GAA-CNTFET *N3*.

- **Write Stability**

The calculation of write stability in the proposed dual-chiralityGAA-CNTFET-5T-SRAM, the transistor ratio is must be minimum by the voltage value of dual-chirality V_{dual_C}. Here, the voltage value of V_{dual_C} is not affect the write operation of proposed model since, the BL is detained as ground.

3.3 Design of Ballistic Wrap Gate CNTFET Based Self-controlled 5T SRAM Cell

The Ballistic wrap gate CNTFET based 5T SRAM cell is designed for smaller power and maximum R/W Assist performance. Here, Ballistic wrap gate CNTFET based 5T-SRAM is designed through self-controllable voltage level (SVL) circuit to diminish leakage current and power, which is shown in Fig. 5. Additionally, the BWG-CNTFET-based 5T-SRAM cell design uses single-ended read and differential write using single-ended write option. Instead of cross-coupled IC, the BWG-CNTFET-5T-SRAM cell uses a transistor that is executed in low threshold device (LVT). For improving cell functionality, pull-up devices are executed using high-threshold (HVT) devices. For hold state, BWG-CNTFET-5T-SRAM cell acts as standard cross coupled latch. For read operation, destructive positive

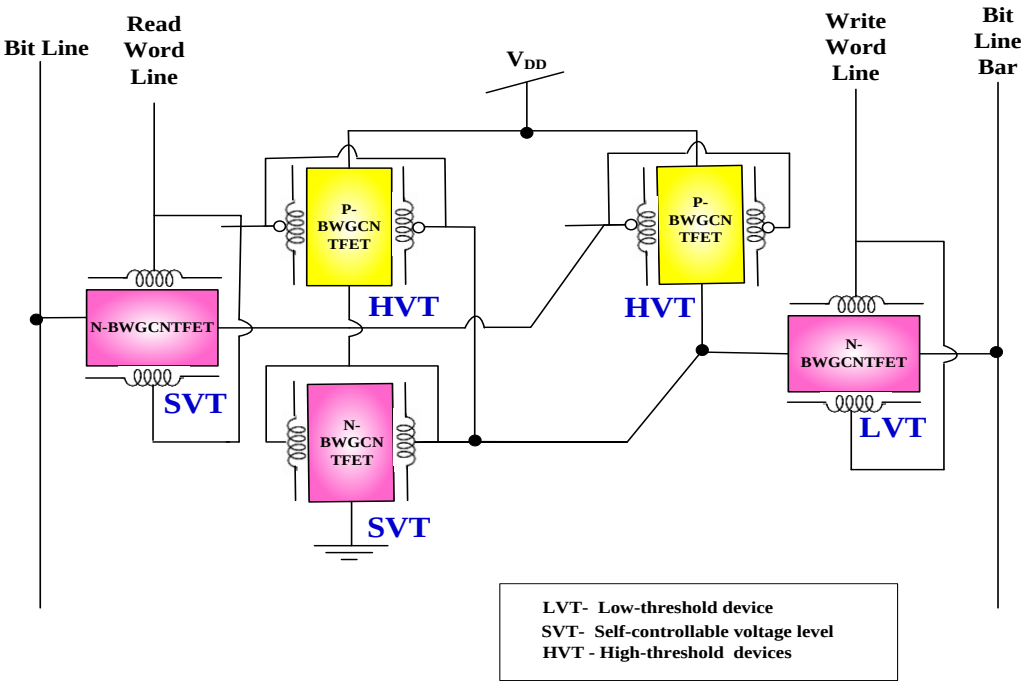

Fig. 5 Block diagram of Ballistic wrap gate CNTFET based self-controlled 5T-SRAM cell.

feedback is removed, so it cause pull-down network lacking makes the cell to flip. Thus, read operation is executed by single-ended operation, which provides slight enhancement on read stability and removes that read-sizing constraint. For write operation, it uses differential write option for single-ended write. Subsequently, performance of proposed BWG-CNTFET based 5T-SRAM cell design are measured in terms of cell area, minimum VDD, Leakage power, R/W access time, leakage current and static noise margin for stability analysis.

The CNTFET is utilized zero band gap metals or semiconductors through finite band gap using wrapping vector. Here, the developed CNTFET involves wrap-gate construction encircling single/an array of semiconducting nanotube through high-k dielectric material for limiting gate leakage current. Additionally, the physical gate width G_w of the Ballistic wrap gate CNTFET transistor is calculated using Eq. (3):

$$G_w = A_P(T_{CNT} - 1) + d_{CNT} + 2W \qquad (3)$$

where, A_P represents the array pitch that is mentioned in uniform manner, T_{CNT} denotes the quantity of nano tubes, $W = 2\lambda$ and d_{CNT} is the diameter of nano tubes.

The proposed Ballistic wrap gate CNTFET employing a single-ended read as well as disparity write option for single-ended write. Modification in circuit removes back gate control of correct AT (N-type BWG-CNTFET) and operating multi-threshold devices are detailed. Additionally, N-type BWG-CNTFET is simulated as LVT device and right BL detained less during the standby model and the read operation model. Consequently, read operations in the model are attained single-ended by left access transistor N-type BWG-CNTFET based on RWL signal. Subsequently, the write operations are obtained differentially through declaring both RWL and WWL. Furthermore, the pull-up devices are processed in the proposed model for enhancing the cell functionality through high-threshold (HVT) devices.

Subsequently, the working procedure of the design is based on three operations that are hold, read, and write, which are detailed as below.

- **Hold operation**

In this section, the proposed BWG-CNTFET-5T-SRAM cell is same with standard cross-coupled latch for holding the trivial state as logical ‘0’. Here, the N-type BWG-CNTFET is turned on by discharging node (*D*) that allows the *Db* node is fully charged to V_{DD}. Consequently, absence of pull-down device is *Db* outcome on robust hold “0” state; but, this can ruthlessly blocks the opposite (hold “1”) state. Thus, (*D*) is charged to V_{DD} and the value *Db* is diminished to V_{SS}. If P-type BWG-CNTFET is turned on when holding (*D*) high, but it seems to be holding *Db* as low. Thus, to achieve stronger leakage current as node *Db* to V_{SS} from V_{DD} to *Db*, stable state is ensured, which are attained by three operations:

a) Executing N-type BWG-CNTFET with double width LVT device.

b) Executing P-type BWG-CNTFET with HVT device.
c) Biasing BL at V_{SS} when writing as '1'.

- **Read operation**

In read operation, the BL access transistors turned on the invasive state that causes less internal data node level, which represent node holding as "0". Increase at level of (*D*) cannot cause cell flip because of the absence of pull-down network at node *Db*. Consequently, read operation is executed in the single-ended (*D*) node that provides an important development under read stability. Then, Read Word Line is declared, that results in the single-ended readout of node (*D*). If (*D*) increases (hold"1" condition), there contains no voltage drops over N-type BWG-CNTFET and the entire voltage level remains unchanged.

If (*D*) value is less (hold "0" condition) then charge is initiating between the bit line and node (*D*) is resulted in "zero" readout. As 5T readout, the voltage level at *D* increases that overdrive voltage of P-type BWG-CNTFET by pull-up of *Db*. Though, node *Db* is left at higher state because it is not an active pull-down network for discharging. The N-type BWG-CNTFET (V_{GS}=*Db*=V_{DD}) faster discharge *D* back to their original state feed via *D* in the falling edge of Read Word Line increases in this effect.

- **Write Operation**

The proposed BWG-CNTFET-5T-SRAM cell uses usual variance write operation, while BL is driven to opposite levels. Consequently, both Write WL and Read WL are emphasized. To guarantee readability, the access transistors (AT) are enabled. This demand basically disables that pull-up path on write by sendoff most of the write operation on pull-up side. The variation increases with decreasing voltage, it restricts the write capacity of the 5T cell, around 700mV. The single-ended read operation of the proposed 5T cell basically eliminates the read size restriction of N-type BWG-CNTFET right access transistor. While, the 5T cell improves the efficacy of pull-up operation via type N BWG-CNTFET, since the node *Db* does not contain a pull-down network to resist it. So, loading BL and asserting Write Word Line simply raises the past threshold voltage of N-BWG CNTFET by enabling the node *Db* pull-down network. This write operation "0" achieves the single end.

The BL is charged and right BL is discharged and both WL are declared. For effectively flip the cell state, *Db* is discharged after switching threshold value of left inverter. While *D* must be charged and it is highly enough to cut off P-type BWG-CNTFET. Topologically, this operation is less robust than 5T cell. Since, the lack of positive feedback requires a high voltage surge that is presented before effective write operation. The right side cell is executed for making sure that positive pull-down leak ratio through hold state "1", with double-width, low-threshold implant for BWG-CNTFET of type N, and HVT implant in type P BWG-CNTFET. Hence, the pull-down path to the right BL is too stronger to pull-up path via P-type BWG-CNTFETs, to guarantee an effective discharge of *Db* even under great variation. Also, "one" write operation may be accomplished at only one end, somewhat degrade the write margin. Certainly, the execution of single-ended write access system does not need structural changes to the cell.

3.3.1 Stability Analysis

It is the important aspect for SRAM design in that traditional static noise margin (SNM) is used. This criterion is more violent for hold and read operation is optimistic for the writing functions.

- **Hold Stability**

The SNM metric is usually employed measurement of SRAM stability, measuring the biggest DC voltage that is used to the inner data nodes of a cell devoid of turning the cell a bit. The SNM metric is optimistic because it emulates an infinite number of non-physical noise sources. An enlarged margin for the condition of hold=0, which have no positive feedback. Subsequently, at condition of hold=1 is maintaining the ratio of leakage current and improved the low voltage. Thus, the value of SNM in hold operation is intrinsically lower that is sensitive for process variations. Consequently, the hold stability demonstrates that the improved robustness in hold 0 conditions and stability of hold 1 condition is inhibited.

- **Read Stability**

In this section, the calculation read SNM (RSNM) as often carried out in the same style as hold operation through BL and WL are tied to V_{DD}. Subsequently, the RSNM metric to proposed BWG-CNTFET-5T-SRAM cell, the improved margin is attained in the result and the N-type BWG-CNTFET assists in holding node (*D*) is high. Additionally, the read SNM measurement for the condition of hold zero demonstrates the robustness. Below extreme mismatch, voltage at node (*D*) is increased at high levels that are enough to weaken P-type BWG-CNTFET in that, the leakage through N-type BWG-CNTFET is pull down at node *Db* and flip the

bit. The ratio between leakage current is culminating after longer duration and it is much longer than lower-frequency read pulse.

- **Write Stability**

The calculation of write SNM is less serial voltage required for driving a bit cell to the mono-stable condition based on writing process. This measurement is more optimistic because it takes infinitely longer writing pulse. The write stability of proposed BWG-CNTFET-5T-SRAM cell measurement is calculated by applying write voltage to both BLs for reducing the asymmetric nature of SRAM cell. Initially consider an infinitely long write pulse too pessimistic for static measurement. Subsequently, the cell trigger point is identified to measure the write margin that changes at each statistical corner. Finally, every runs are successful because of the improved write-ability of BWG-CNTFET-5T-SRAM cell design.

4 Results and Discussion

Here, the performance of self-controlled 5T-SRAM cell corresponding to read/write assist technique using DC-GAA-CNTFET and BWG-CNTFET technologies are evaluated. The proposed 5T-SRAM designs are simulated utilizing HSPICE simulation tool. The simulations are performed at PC using Intel Core i5, 2.50 GHz CPU, 8GB RAM, Windows 7. The performance analyses of proposed 5T- SRAM cell related to read or write assist technique using DC-GAA-CNTFET technology is compared to DG-CNTFET [25] and state-of-art method. Similarly, the performances of proposed 5T- SRAM cell related to R/W assist method using BWG-CNTFET approach is compared with Reduced Power with Enhanced Speed (RPES) approach [27], and state-of-art method.

4.1 Performance Metrics

Performance measures like area, read delay, read power, write delay, write power, read speed, write speed, PDP, and along with SNM are examined to identify the efficiency of the proposed models.

4.1.1 Average Read/Write (R/W) Power Consumption

The average R/W Power Consumption of the proposed 5T-SRAM designs are calculated with Eq. (4):

$$P_{avg} = \lambda V_{DD}^2 (C_L . C_f) \quad (4)$$

where, clock frequency of the model is represented as C_f, the load capacitance is denoted by C_L, the activation factor is represented as λ and the supply voltage is denoted as V_{DD}.

4.1.2 Calculation of SNM

The SNM of SRAM cell consist of less amount of noise voltage at storage terminals of SRAM is needed to flip cell state.

- **Read SNM**

The read SNM is computed by means of read voltage transfer characteristic (VTC) that is determined utilizing extensive dc voltage in node “A”, at the same time as scrutinizing the voltage at node “B”. It is subsequently determined derived from the prevalent square, it fits read butterfly curve inside the lobes.

- **Write SNM**

This is computed by means of the write VTC that is determined utilizing extensive dc voltage in node “A”, at the same time as scrutinizing the voltage at node “B”. It is subsequently determined derived from the prevalent square, it fits write butterfly curve inside the lobes.

4.2 Simulation Results

The simplest technique of measuring noise margins is to plot the butterfly curve that outcomes voltage transfer curve (VTC) of two cross-coupled inverters. VTC of one inverter is plotted through inverse VTC of second inverter to get butterfly curve. The Read SNM butterfly diagram is equal to SNM with few changes in that the ATs are turned on for read mode and from this the value of Read SNM is decremented as SNM. Though, the butterfly diagram for Write SNM is totally dissimilar data is totally overwritten under this state using novel values. This is the reason why the Write SNM value refers maximum between the entire noise margins. It may be computed by calculating the longest square side that may be placed among the reflected butterfly curves. Also, power consumption, area and delay values of proposed 5T-static random access memory designs are illustrated. Here, the simulation outcomes of current, voltage and butterfly curve for the DC-GAA-CNTFET based 5T SRAM Cell and BWG-CNTFET based 5T-SRAM are mentioned.

Figure 6 shows that the current graph of proposed Dual-Chirality GAA CNTFET fed 5T-SRAM Cell design. In this graph, the current flow in bit line is represented as i(vBL), the

current flow in word line is represented as i(vWL), and the supply voltage is denoted as i(VDD), which are calculated based on time.

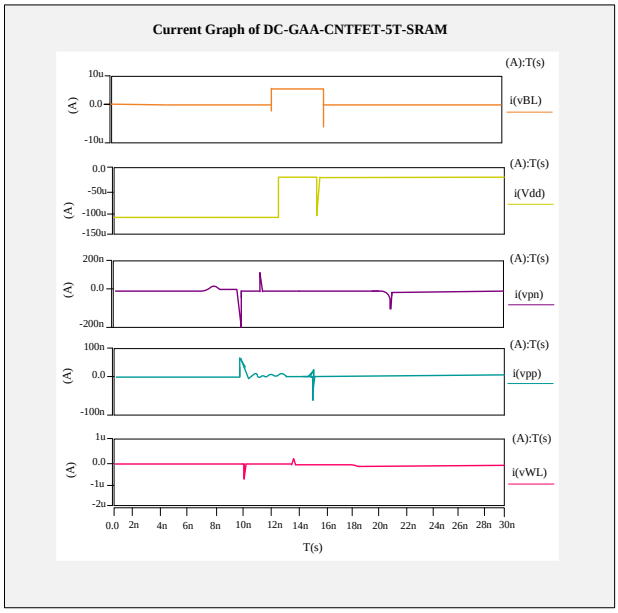

Fig. 6 Current graph of proposed Dual-Chirality GAA-CNTFETs based 5T-SRAM Cell design.

Figure 7 show that the voltage simulation graph of the proposed Dual-Chirality Gate all around CNTFET fed 5T-SRAM Cell design. The voltage in the bit line is represented as v(BL), the voltage in word line is represented as v(WL), the supply voltage refers (V_{DD}), voltage at node A refers v(D), and voltage at node B is mentioned as v(Db) which are calculated based on time.

Figure 8 show that butterfly curve of proposed Dual-Chirality Gate all around CNTFET fed 5T-SRAM Cell design.

Figure 9 show that current graph of proposed BWG-CNTFET based 5T-SRAM Cell design. In this graph, the current flow in bit line is represented as i(vBL), the current flow in word line is represented as i(vWL), and the supply voltage is denoted as i(V_{DD}), which are calculated based on time.

Figure 10 show that voltage graph of proposed BWG-SRAM based 5T-SRAM Cell design. In this graph, the voltage in the bit line is represented as v(BL), the voltage in word line is represented as v(WL), the supply voltage is denoted as v(V_{DD}), voltage at node A is denoted as v(D), and the voltage at node B is mentioned as v(Db) which are calculated based on time.

Figure 11 show that butterfly curve of proposed BWG-CNTFET fed 5T-SRAM cell design.

4.3 Comparison Result of DC-GAA-CNTFET-5T-SRAM

Here, comparative analysis of DC-GAA-CNTFET model is explained. The performance analysis of proposed DC-GAA-CNTFET 5T-SRAM design is likened with DG CNTFET-6T-SRAM [25] and state-of-art method as ED-GAA-CNTFET-5T-SRAM.

Figure 12 depicts the performance analysis of area with different method. The area of proposed DC-GAA-CNTFET 5T-SRAM method provides 33.33% and 12.66% lower area related to existing methods as DG-CNTFET 6T-SRAM and ED-GAA-CNTFET-5T-SRAM respectively.

Figure 13 portrays performance analysis of R/W delay with different method. For read operation, the proposed DC-GAA- CNTFET-5T- static random access memory method provides 11.31% and 51.47% lower read delay related to DG-CNTFET 6T-SRAM and ED-GAA-CNTFET-5T- SRAM methods respectively. For write operation, the proposed DC-GAA-CNTFET-5T-SRAM method provides 44.44% and 26.33% lower write delay is related to DG- CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-static random access memory respectively.

Figure 14 portrays performance analysis of R/W power with different method. For read operation, the proposed DC-GAA-CNTFET-5T-SRAM method provides 36.12% and 45.28%, lower read power compared with DG-CNTFET-6T-static random access memory and ED-GAA-CNTFET-5T-SRAM methods respectively. For write operation, the proposed DC-GAA-CNTFET-5T-Static Random Access Memory method provides 34.5% and 22.41% lower write power compared with DG-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-Static Random Access Memory methods respectively.

Figure 15 portrays performance of read speed and writes speed with different method. For read operation, proposed DC-GAA-CNTFET-5T-SRAM method provides 49.20% and 54.53% higher read speed compared with existing methods like DG-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM methods respectively. For write operation, proposed DC-GAA-CNTFET-5T-SRAM method provides 44.5% and 32.11% higher write speed compared with existing methods like DG-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM respectively.

Figure 16 shows that performance of PDP with different method. A PDP of proposed DC-GAA-CNTFET-5T-SRAM method provides 46.3% and 39.67% lower PDP related to existing methods like DG-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM correspondingly.

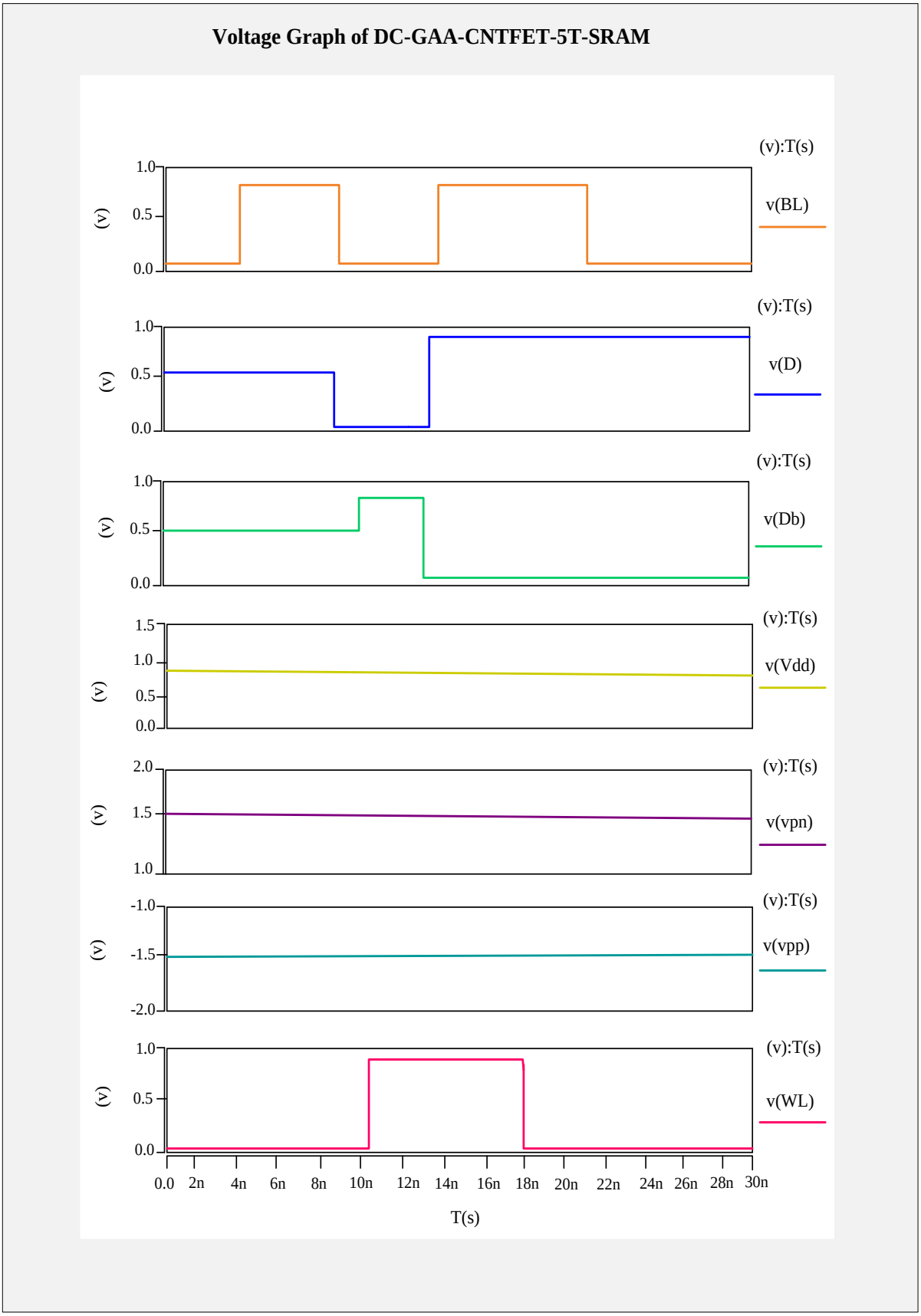

Fig. 7 Voltage graph of proposed Dual-Chirality GAA-CNTFETs based 5T-SRAM Cell design.

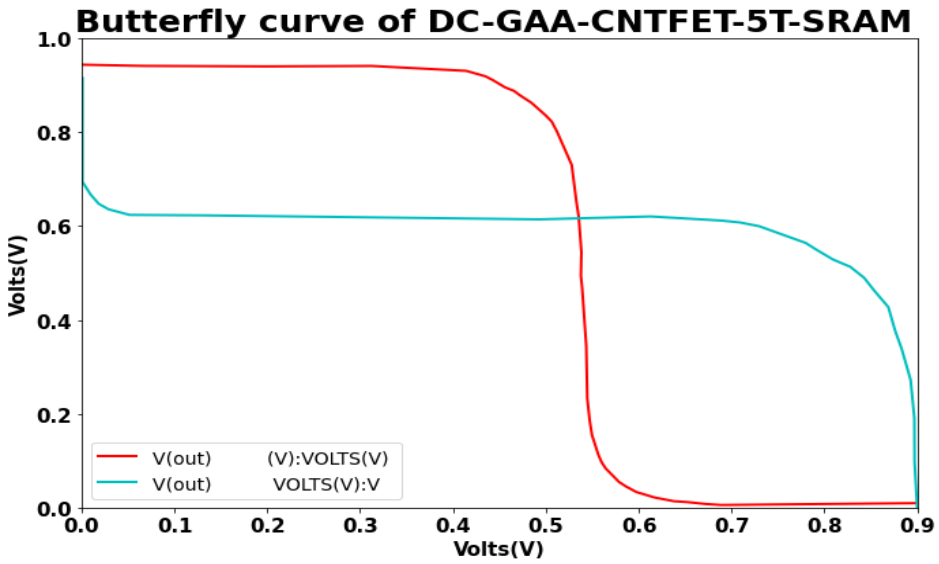

Fig. 8 Butterfly curve of proposed DC-GAA-CNTFET based 5T-SRAM Cell design.

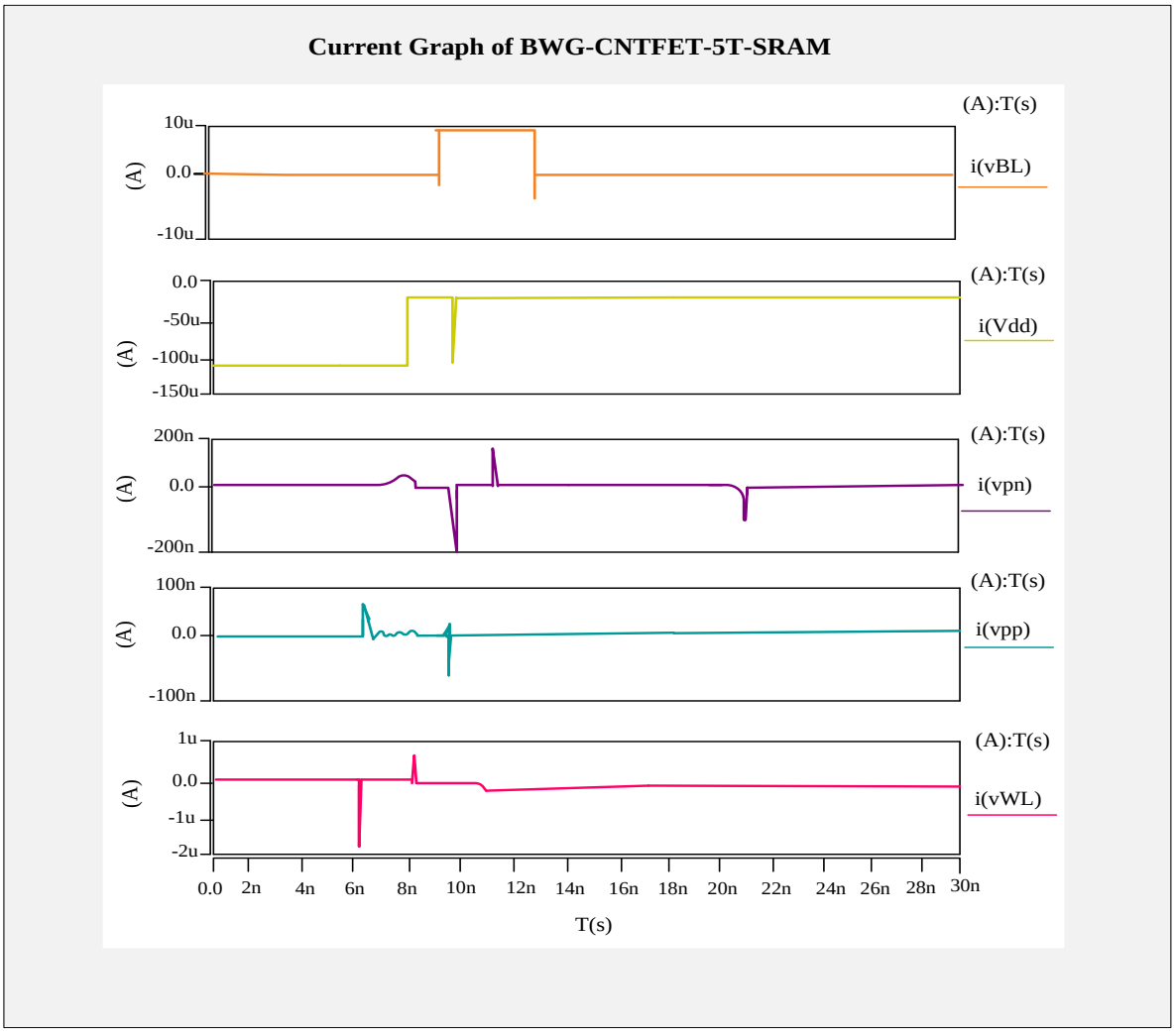

Fig. 9 Current graph of proposed Dual-Chirality GAA-CNTFETs based 5T-SRAM Cell design.

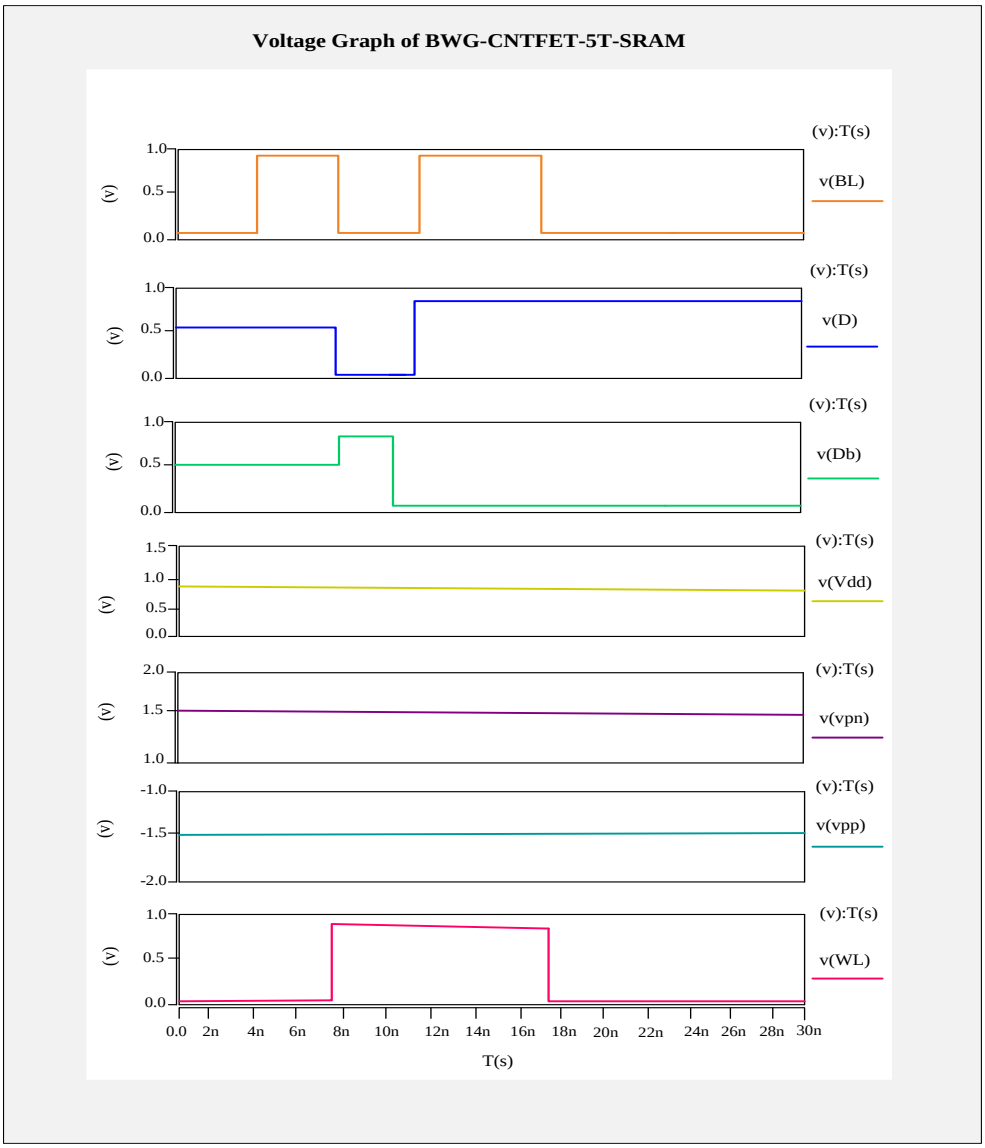

Fig. 10 Voltage graph of proposed BWG-CNTFET based 5T-SRAM Cell design.

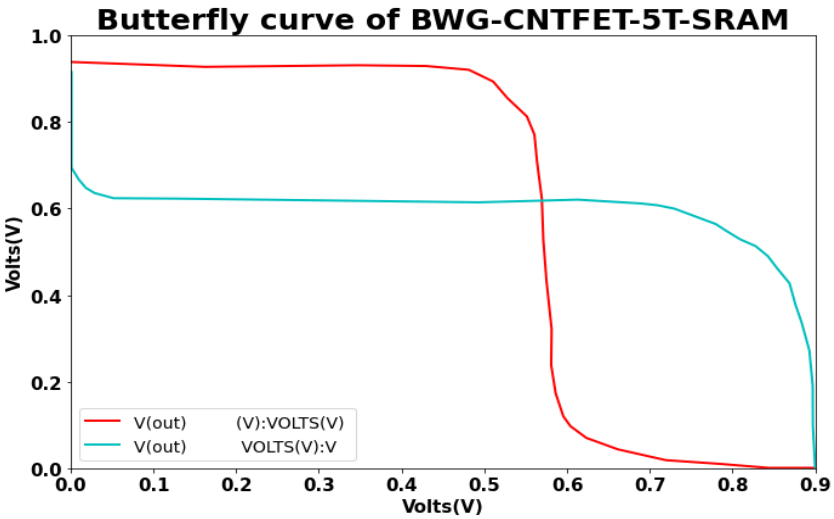

Fig. 11 Butterfly curve of proposed BWG-CNTFET based 5T-SRAM Cell design.

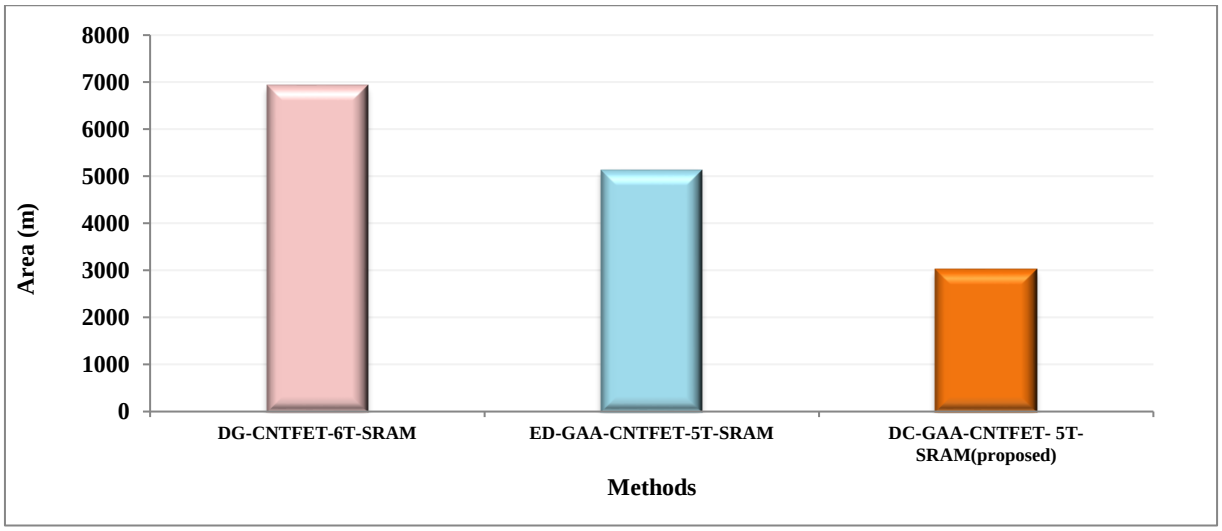

Fig. 12 Performance analysis of area with different method.

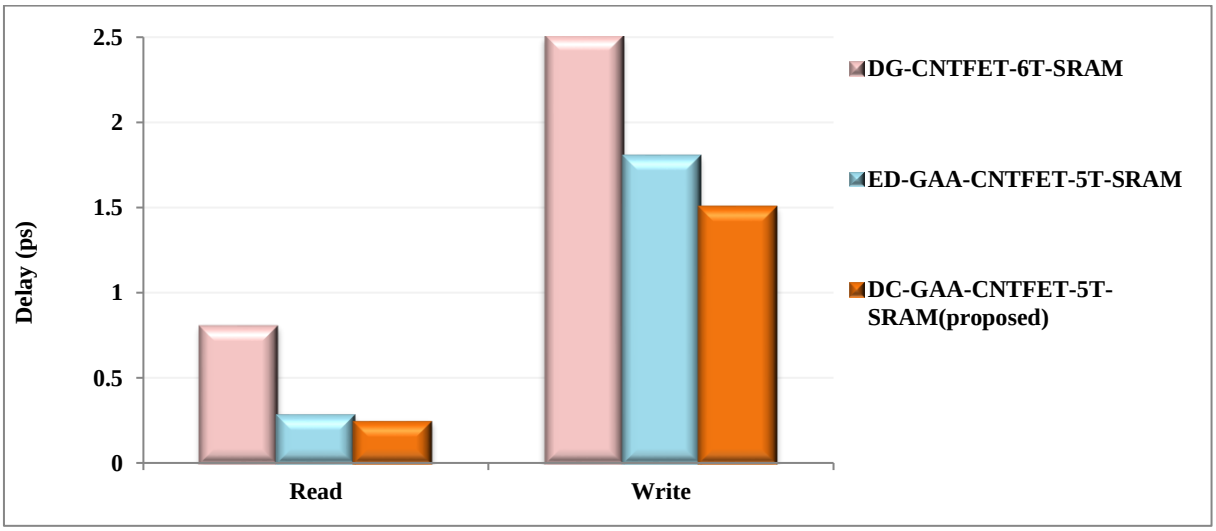

Fig. 13 Performance analysis of read delay and write delay with different method.

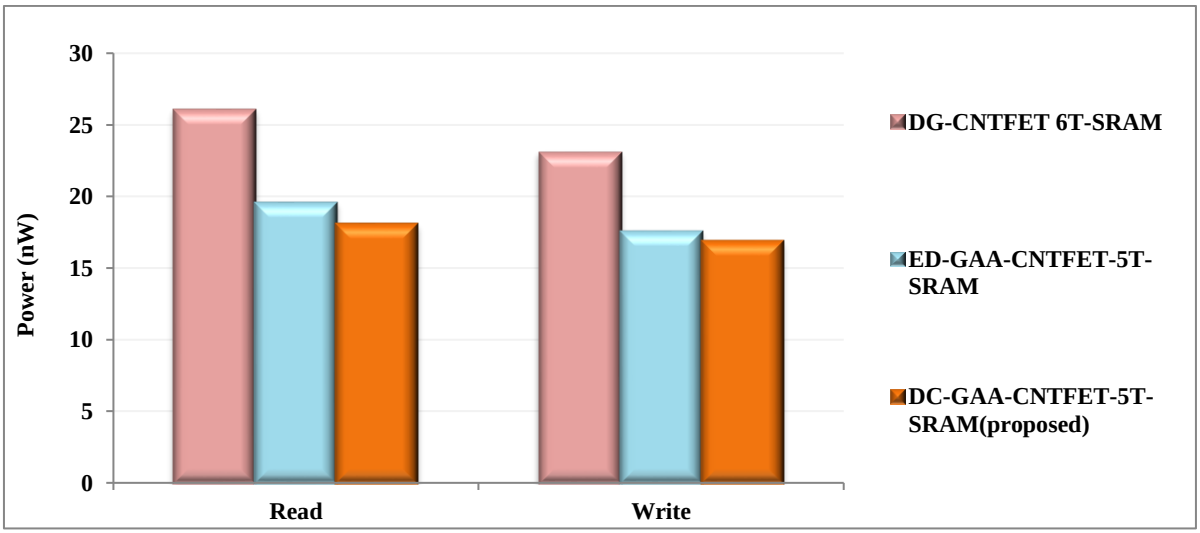

Fig. 14 Performance analysis of read and write power with different method

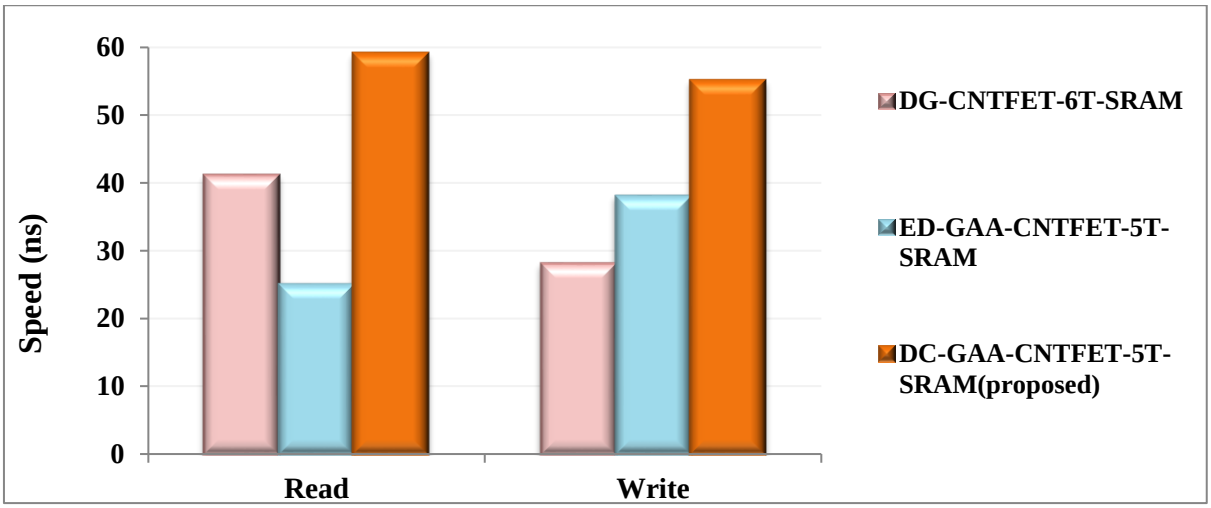

Fig. 15 Performance analysis of read and write speed with different method.

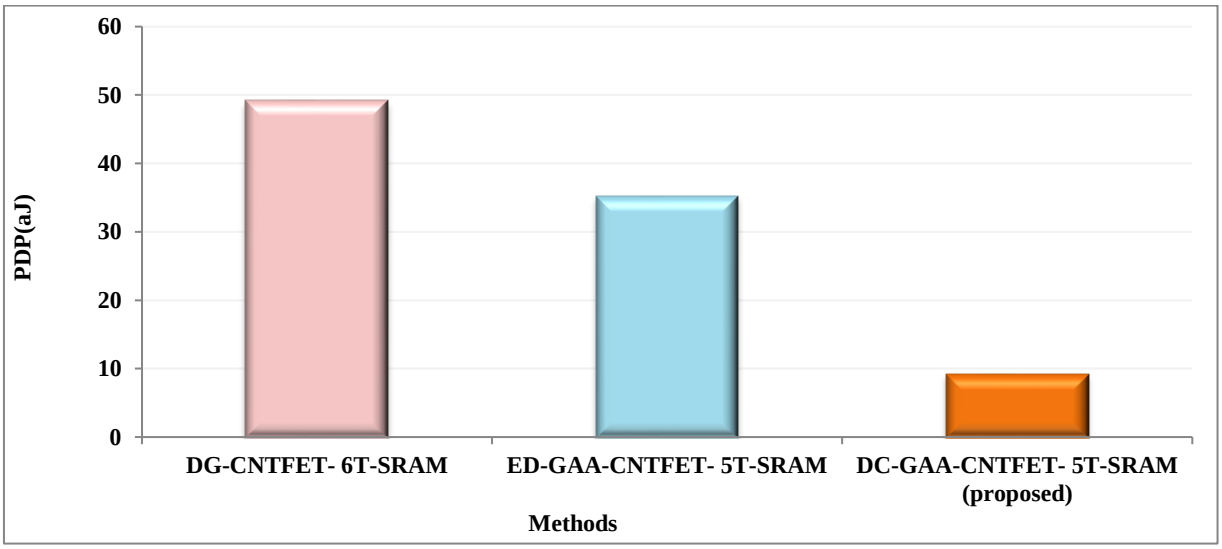

Fig.16 Performance analysis of PDP with different method.

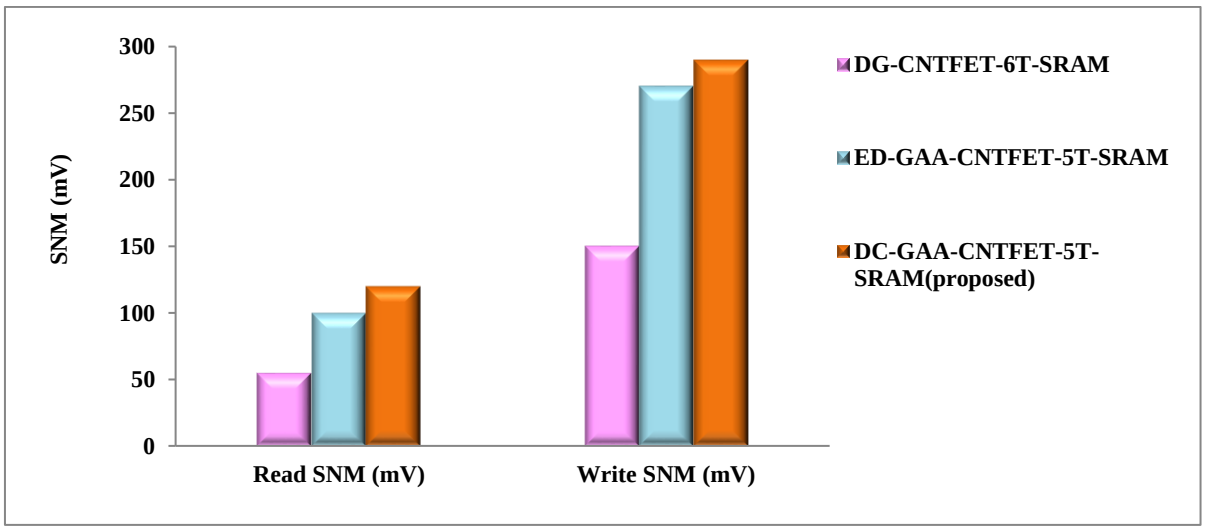

Fig. 17 Performance analysis of SNM with different method.

The performance of SNM with different approaches is depicted in Fig. 17. For read operation, proposed DC-GAA-CNTFET-5T-SRAM method provides 37.4% and 15.3% higher read SNM related to DG-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM respectively. For write operation, the proposed DC-GAA-CNTFET-5T-SRAM method provides 35.8% and 12.09% higher write SNM related to DG- CNTFET-6T-SRAM and ED-GAA- CNTFET -5T-SRAM methods respectively.

4.4 Comparison Result for BWG-CNTFET-5T-SRAM Design

Here, the comparative analysis of BWG- CNFET-5T-SRAM model is explained. The performance analysis of proposed BWG-CNTFET-5T-SRAM design is likened to reduced power with enhanced speed (RPES) approach [27], and ED-GAA-CNTFET-5T-SRAM method.

Figure 18 depicts the performance analysis of area with different method. The area of the proposed BWG-CNTFET-5T-SRAM method provides 29.66% and 43.5% lesser area related to existing methods such as RPES-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-Static random access memory respectively.

Figure 19 portrays that performance analysis of read delay and writes delay with different method. For read operation, the proposed BWG-CNTFET-5T-SRAM method provides 56.67% and 45.64% lower read delay compared with RPES-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM methods respectively. For write operation, the proposed BWG-CNTFET-5T-SRAM method provides 45.53% and 38.77% lower write delay compared with RPES- CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM methods respectively.

Figure 20 portrays that performance analysis of read and writes power with different method. For read operation, the proposed BWG-CNTFET-5T-SRAM method provides 58.4% and 56.75% lower read power related to existing approaches such as RPES-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM respectively. For write operation, the proposed BWG-CNTFET-5T-SRAM method provides 49.66% and 28.56% lower write power compared with RPES-CNTFET 6T-SRAM and ED-GAA-CNTFET-5T-SRAM.

Figure 21 portray performance of read speed and write speed with different method. For read operation, the proposed BWG- CNTFET-5T-SRAM method provides 45.57% and 37.54% higher read speed likened with RPES-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM respectively. For write operation, the proposed BWG-CNTFET-5T-SRAM method provides 49.35% and 68.23% higher write speed likened to RPES-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM methods respectively.

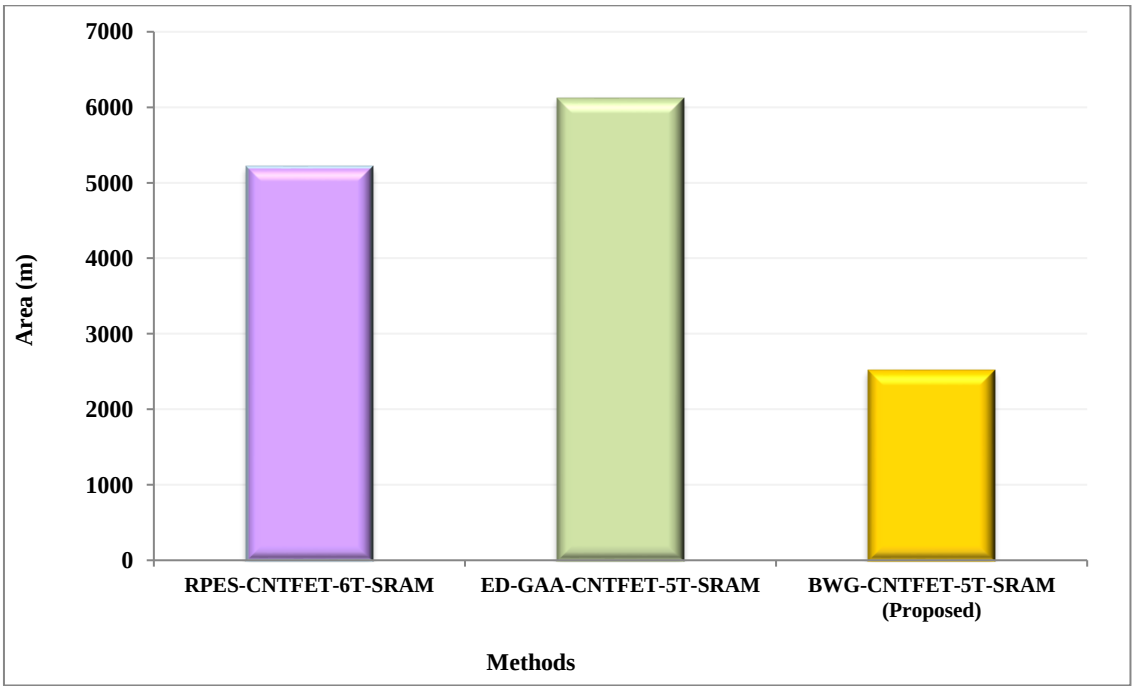

Fig. 18. Performance analysis of area with different method.

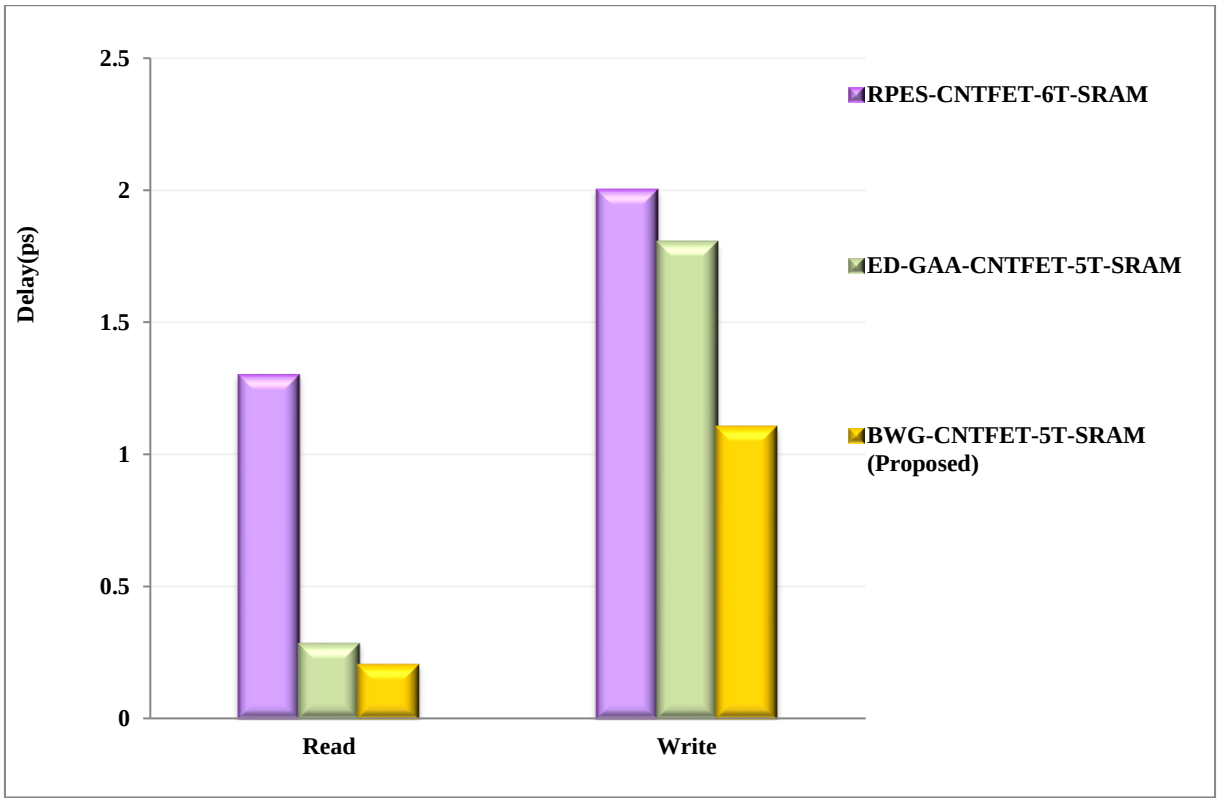

Fig. 19 Performance analysis of read and write delay using different method.

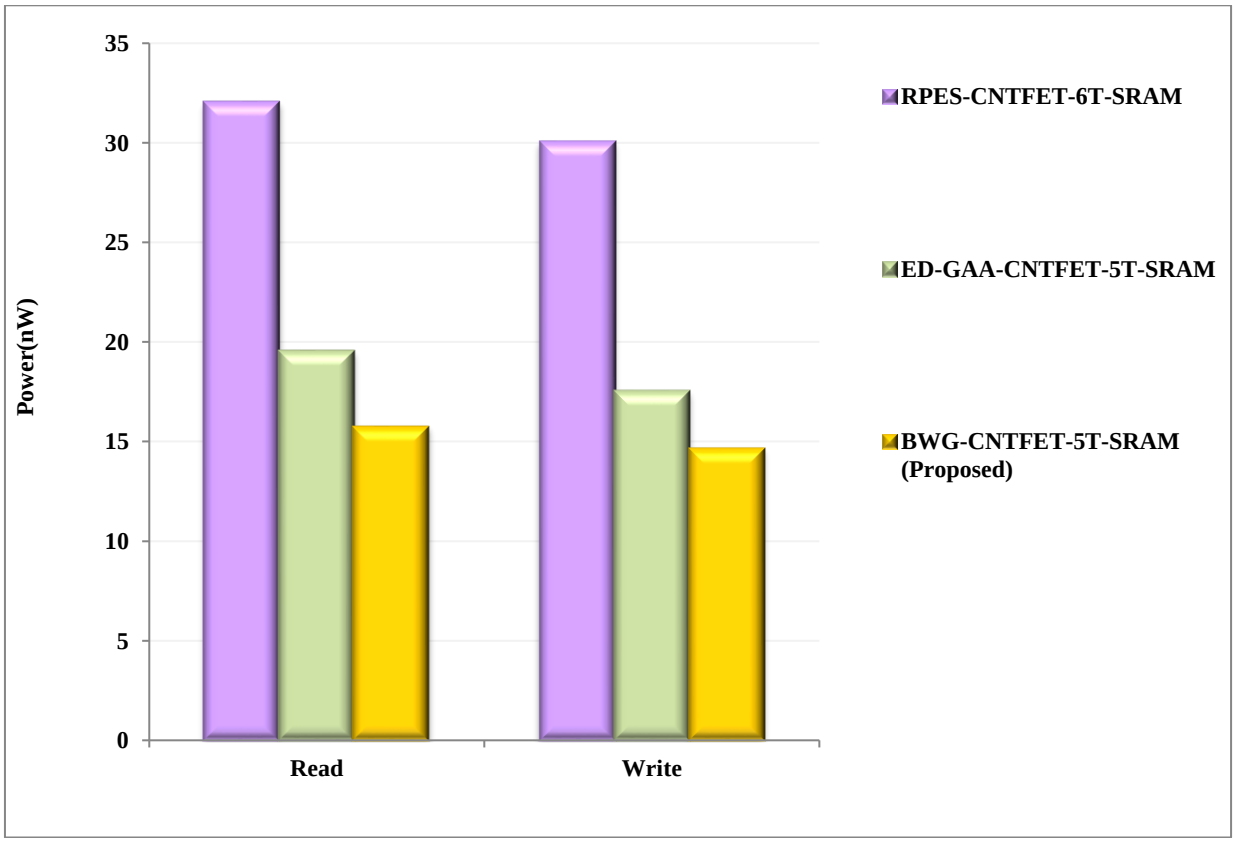

Fig. 20 Performance analysis of read and write power with different method.

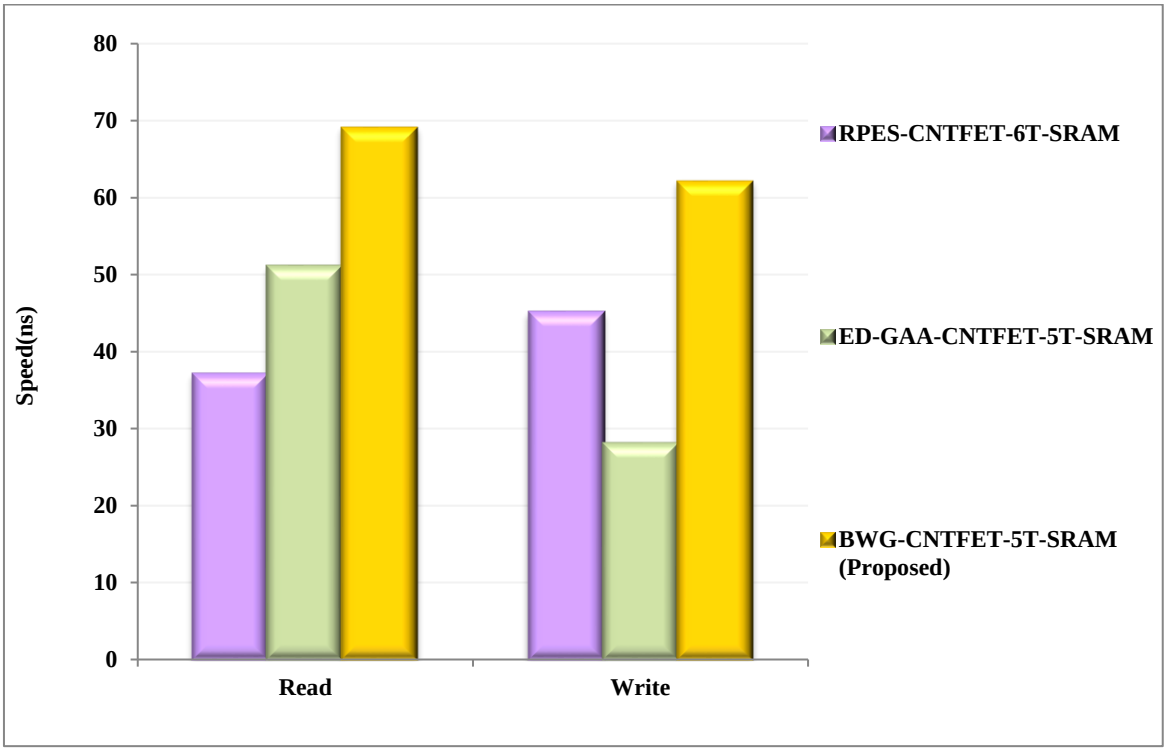

Fig. 21 Performance of read speed and write speed with different method.

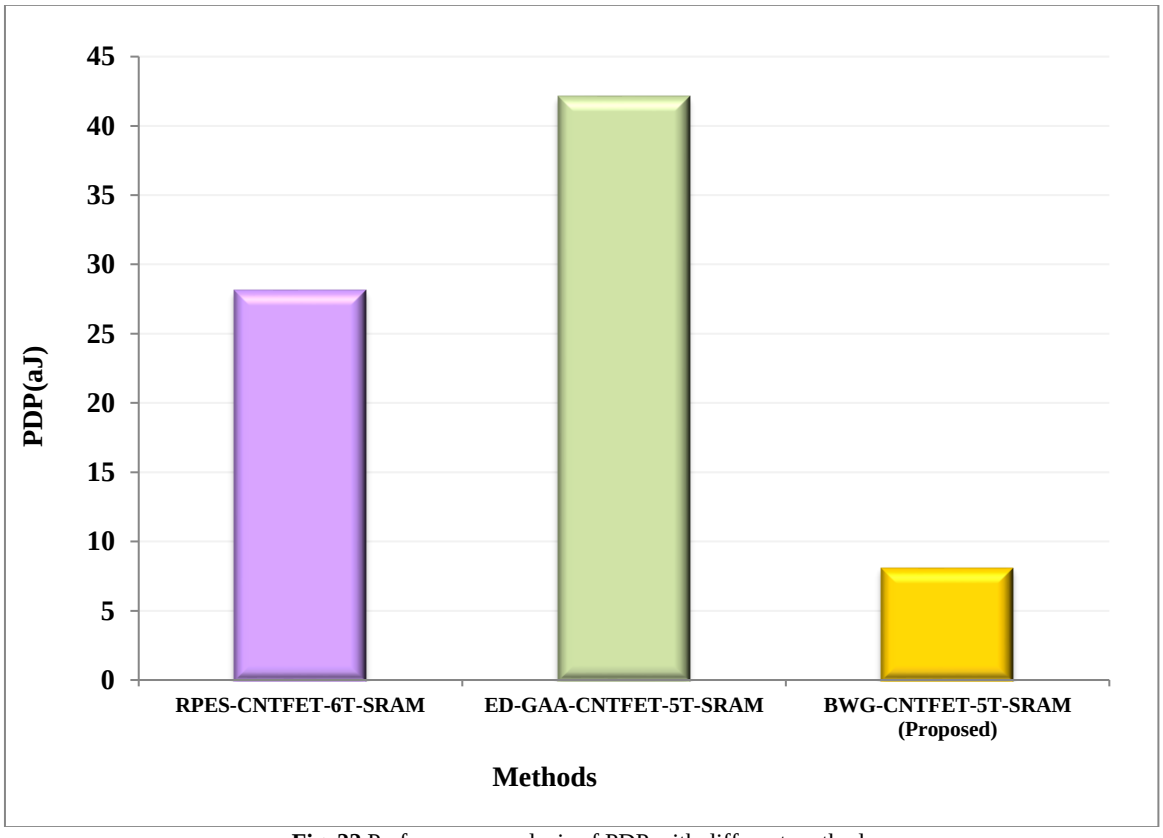

Fig. 22 Performance analysis of PDP with different method.

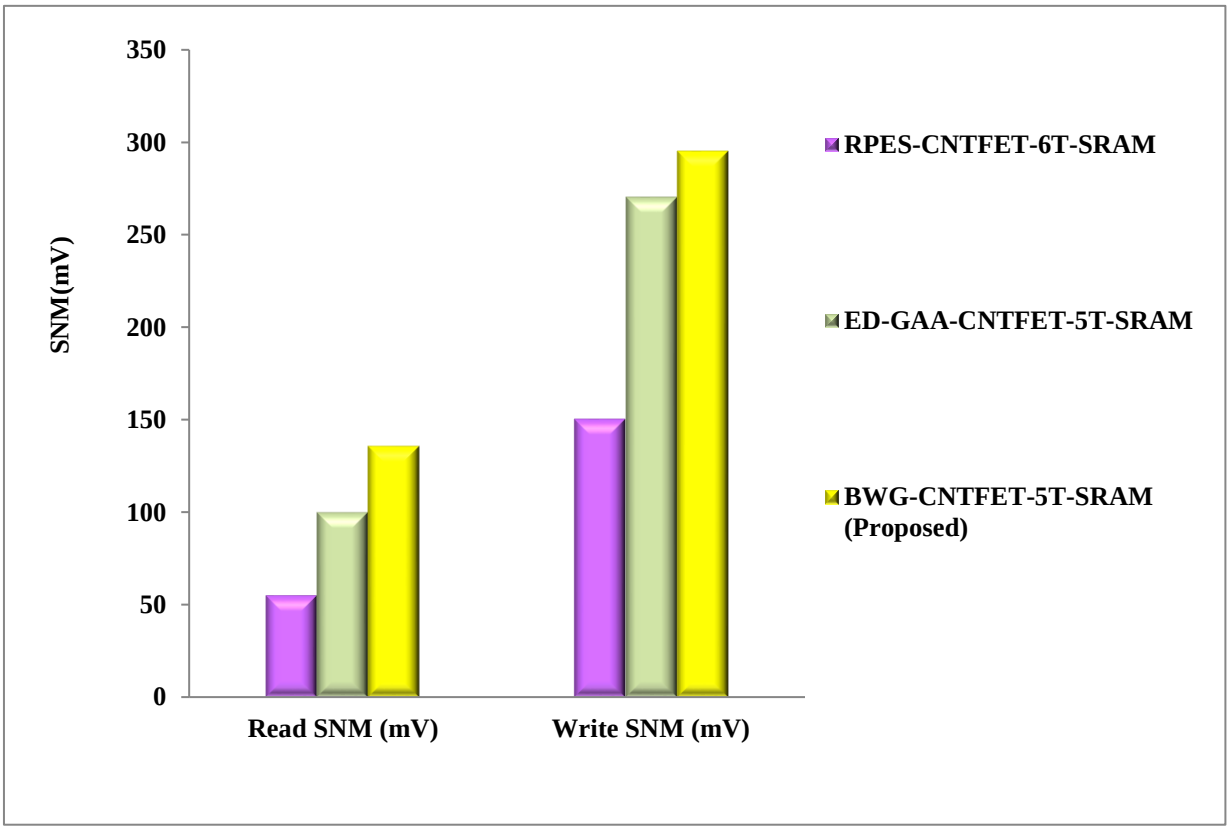

Fig. 23 Performance of SNM with different method.

Table 1 Performance Comparative analysis of proposed designs with existing methods.

Parameters		DG CNTFET-6T-SRAM	RPES-CNTFET-6T-SRAM	ED-GAA-CNTFET-5T-SRAM	DC-GAA-CNTFET-5T-SRAM (Proposed 1)	BWG-CNTFET-5T-SRAM (Proposed 2)
Area (m)		6900	5200	5100	3000	2500
Delay (ps)	Read	0.8	1.3	0.28	0.24	0.2
	Write	2.5	2	1.8	1.5	1.1
Power (nW)	Read	26	32	19.5	18	15.7
	Write	23	30	17.5	16.8	14.6
Speed (ns)	Read	41	37	25	59	69
	Write	28	45	38	55	62

Figure 22 portrays performance of PDP with different method. The PDP of proposed BWG-CNTFET-5T-SRAM method provides 36.21% and 59.06% lower PDP related to RPES- CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM methods correspondingly.

Figure 23 portrays performance of SNM with different method. For read operation, the proposed BWG-CNTFET-5T-SRAM method provides 35.32% and 12.7% higher read SNM compared with RPES-CNTFET -6T-SRAM and ED-GAA-carbon nanotube field effect transistors-5T-SRAM respectively. For write operation, the proposed BWG-CNTFET-5T-SRAM method provides 45.8% and 15.6% higher write SNM related to RPES-CNFETs -6T-SRAM and ED-GAA-CNTFET-5T-SRAM methods respectively.

Table 1 shows that the Comparative analysis of proposed DC-GAA-CNTFET 5T SRAM model Performance with existing approaches such as DG-CNTFET-6T-SRAM, RPES-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM methods respectively.

Also, the comparative analysis of proposed designs like DC-GAA-CNTFET-5T-SRAM and BWG-CNTFET-5T-SRAM performances are analyzed and detailed in table 1. The BWG-CNTFET-5T-SRAM (proposed 2) design has attained 12.45% lower area, 0.4% lower read delay, 0.29% lower write delay, 3.67% lower read power, 2.98% lower write power, 11.76% higher read speed, 13.06% higher write speed, 15.73% higher read SNM, 4.36% higher write SNM, 2.45% lower PDP than the DC-GAA-CNTFET-5T-SRAM (proposed 1) design. Thus, the parameters like area, delay, power, speed, PDP, and static noise margin of BWG- CNTFET -5T-SRAM (proposed 2) is slightly improved than DC-GAA-CNTFET-5T-SRAM (proposed 1) design.

5 Conclusions

In this paper, Dual-Chirality Gate all around (GAA) CNTFET and Ballistic wrap gate CNTFET based self-controlled 5T SRAM cell designs are proposed for enhancing the read/write assist process and diminishing the power utilization. Here, the proposed Dual-Chirality GAA-CNTFET based 5T SRAM consists of 2 cross-coupled inverters with one access transistor is linked through BL and WL. Additionally, BWG-CNTFET 5T-SRAM cell is considered to improve R/W process through low power. Therefore, the proposed Dual-Chirality GAA-CNTFET and BWG-CNTFET 5T SRAM cell designs are utilized to decrease leakage current and power improved the read and write assist processes. Thus, the proposed designs is related to existing approaches in terms of area, delay, power, speed, power delay product and static noise margin. Hence, the proposed Dual-Chirality GAA-CNFET-5T-SRAM cell design attains 33.33%, 12.66% lower area, 49.20%, 54.53% higher read speed, 44.5% , 32.11% higher write speed, and 46.3%, 39.67% lower PDP than

DG-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM methods. Similarly, the proposed BWG-CNTFET-5T-SRAM cell design has attained 29.66%, 43.5% lower area, 45.57% , 37.54% higher read speed, 49.35%, 68.23% higher write speed, 36.21%, and 59.06% lower PDP than RPES-CNTFET-6T-SRAM and ED-GAA-CNTFET-5T-SRAM methods respectively.

Intellectual Property

The authors confirm that they have given due consideration to the protection of intellectual property associated with this work and that there are no impediments to publication, including the timing to publication, with respect to intellectual property.

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CRediT Authorship Contribution Statement

G. S. Kumar: Conceptualization, Methodology, Writing- Original draft preparation. **G. Mamatha:** Supervision.

Declaration of Competing Interest

The authors hereby confirm that the submitted manuscript is an original work and has not been published so far, is not under consideration for publication by any other journal and will not be submitted to any other journal until the decision will be made by this journal. All authors have approved the manuscript and agree with its submission to “Iranian Journal of Electrical and Electronic Engineering”.

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