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Research Paper

A Novel High-Linearity LNA based on Post Distortion and CDS Techniques for UWB Radar

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Abstract: By increasing the transceiver devices within the 3.1 to 10.6 GHz frequency band, the interferers and strong blockers from different equipment degraded the main received signals, so linearity performance becomes more notable. In this paper, a two-path low noise amplifier (LNA) is proposed for satisfying the overall efficiency of the Ultra-wideband (UWB) radar used in vital sign detection, precise indoor localization, and high data rate wireless communications. A novel high linear circuit is recommended based on Complementary Derivative Superposition (CDS) and Post Distortion (PD) techniques. High pass filter and inductive source degeneration structured input impedance matching. Post layout results of the designed UWB-LNA in 180-nm CMOS represented the average of third-order Intercept Point (IIP3) is 8.1 dBm, S21 is 11 dB and, S11 is below -10 dB. The minimum noise figure (NF) is 3.11 dB. The circuit draws 12.7 mA at 1.4-V. The chip area is 930 µm × 1090 µm. The proposed design in this work exhibits higher FOM compared to similar LNAs, It is clear, high-linearity performance in total bandwidth is an advantage compared to recent articles.

Keywords: Linearity, Low-noise Amplifier, Ultra-wideband, Post Distortion.

1 Introduction

THROUGH-WALL detection radar, high data rate communication, 5G communication system, and software-defined radio (SDR) applications usually operate within the 3.1 to 10.6 GHz Bandwidth. The interactions of numerous types of signals should consider for designing a receiver [1]-[5]. Nowadays, the demand for connected devices in the industry and smart homes has increased dramatically. The operating frequency for UWB technology interferes with the devices, and signal degradation could concern manufacturers. In this regard, increasing the linearity of the receiver is a reliable solution to improve the system performance [6], [7].

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The MOSFETs have low current dissipation, high-frequencies operation, support of the high speed of service, and the system on chip integration which are the most desirable candidate for the Radio Frequency (RF) application [8], [9]. The LNA is the critical part of the RF front-end receiver adjusting the linearity and the noise characteristics. Linearity due to the existing strong narrow-band interferes and intermodulation distortion is measured by the IIP3 parameter, used to compare different receivers [10]-[12]. A two-pass structure is a scheme for modifying the LNA to achieve good gain, low NF, and wideband impedance matching [13]. It is practically impracticable to get a policy to accomplish an utterly acceptable efficiency, especially when high linearity is more attractive[14].

The CMOS LNA based on inverter cells was analyzed in [15], and tow-pass LNA based on the inverter is reported in[16]. This structure works at a lower X band and has low IIP3; also, the circuit was verified by schematic simulation. A wideband CMOS-LNA based on complementary push-pull is fabricated in 65-nm with 5.5 dBm of IIP3, but the

maximum operation frequency of this LNA is 1.6 GHz [17]. A LNA based on current-reused CDS is fabricated, which operates at 2.5 GHz applications with IIP3 of 3.2 dBm [18]. Also, a two-pass CMOS-LNA is fabricated for sub-11 GHz application [13], but IIP3 is -9.1 dBm. In [19], a double Common Source (CS) structure (complementary form) is designed for sub-12.6 GHz, in which linearity is not analyzed, and IIP3 is -4.7 dBm.

The main drawbacks of the mentioned papers are linearity performance, and constraint on the bandwidth ordered. Looking for the performance of the tow-path LNA, it can be seen that the linearization technique has not been applied to this structure. Technique CDS has the feature that adjustment IIP3 is done by tuning the bias and size of NMOS and PMOS[20]. Also, linearization is developed by applying the PD method to the output, and there are no matching problems [21]. To solve the impedance matching problem in wideband receivers, the LC filter helps the input matching network [22].

LNA topology based on simultaneous noise and distortion cancellation is another unique solution[23]. In this regard, a novel UWB-LNA base on a two-path structure was proposed to obtain high linearity over the desired band. The new design combines the CDS stage (plotted in Fig. 1) and CS topology, followed by the PD technique. The LNA has high IIP3 (maximum is 12.65 dBm), tolerable power consumption, and moderate NF from the post-layout simulation. The paper will be explained as follows: The circuit operation is detailed in section 2. Characteristics such as linearity, gain, impedance matching, and noise are analyzed in section 3. Post-layout results are discussed in section 4. Eventually, the conclusion is studied in section 5.

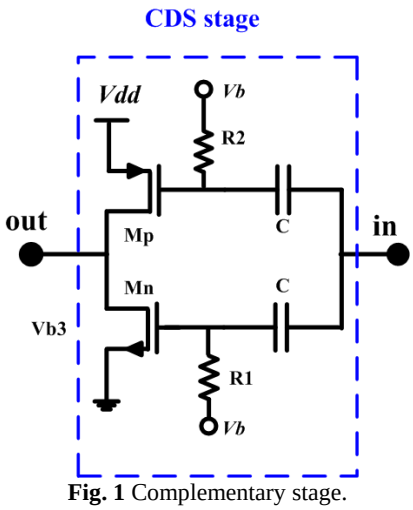

Fig. 1 Complementary stage.

2 Circuit Consideration

The high-performance LNA is a significant challenge in UWB IR radar, UWB Indoor Position Location Systems (IPLS), frequency-division duplex (FDD) mobile communications, 5G, and Cognitive Radio (CR) applications [24]-[27]. Optimal performance with high linearity can be a specific point for designed LNA. Therefore, in the proposed CMOS-LNA, increasing the linearity in the whole frequency range is one of the main intentions. The circuit schematic of the two-path UWB-LNA is shown in Fig. 2.

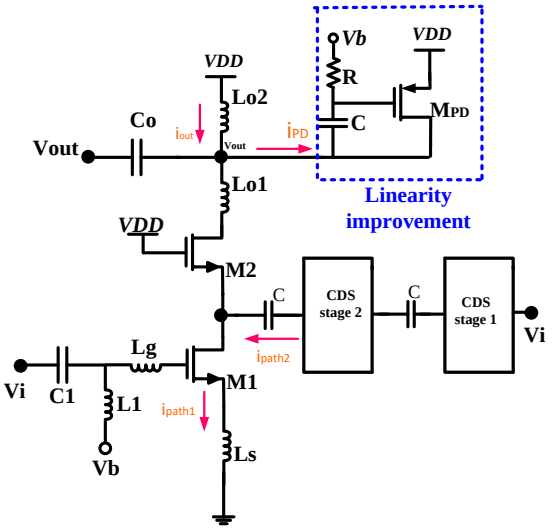

Fig. 2 Proposed two-path UWB LNA.

The circuit has two paths to overcome the nonlinearity and input impedance matching. We define the primary path and secondary path for the CS and CDS stages, respectively. According to Fig.1, CDS stages can eliminate the nonlinearity terms of PMOS and NMOS[11], [22], so the secondary path is utilized for improving the linearity. This path includes M_{n1} and M_{p1} transistors which made stage one, stage two is made with M_{n2} and M_{p2} transistors. However, this path has poor impedance matching. In this regard, inductive degenerated (L_s) CS configuration (M_1) based on LC filter is applied to the primary path, resulting in wideband matching at the LNA.

The output current of CDS stages and the CS structure is still nonlinear. As it is known, the post distortion technique is an excellent method to enhance linearity. Therefore, in the output node of the LNA, the transistor M_{PD} is employed to promote the IIP3 in the whole frequency band. By employing the above procedure, enhanced linearity can be obtained in a two-path UWB-LNA. Post-layout

results validate its effectiveness, which overcomes the limitation of the usual linearized LNAs.

3 Key Performance Analysis

To better understand the performance of the proposed LNA, several key parameters, including linearity, gain, input patching, and noise, will be theoretically investigated. By accessing the theoretical relationship between the output parameters and the parts of the proposed structure, it is possible to predict the impact of each part on the overall performance of the structure. As a result, we can design the desired structure.

3.1 Linearity Performance

Interferers and intermodulation degraded the performance of an LNA in wideband systems. So highly linear transceivers have sparked work on linearizing LNAs. One of the linear LNA topologies that have been widely reviewed is the Derivative Superposition (DS) method. Modified DS (MDS) and Complementary DS (CDS) are other art to increase the IIP3[20], [28], [29]. In the present study, the UWB structure realizes considerable IIP3 by having a two-path strategy based on CDS configuration. N-type and P-type MOSFET pairs are connected for partial distortion cancellation in the second path. For high linearity LNA, a novel CDS configuration based on the PD method was proposed. The small-signal relation of the current of the MOSFET and v_{gs} as the non-linear element is stated as the following [30]:

$$i_{ds} = g_m v_{gs} + \frac{g'_m v_{gs}^2}{2!} + \frac{g''_m v_{gs}^3}{3!} + \dots \quad (1)$$

In Eq. (1) amount of g'_m is the second derivation of DC current, g''_m is second-order derivatives of the transconductance (g_m). Further higher order distortions are neglected because they can be easily filtered out. For high linearity LNA, g''_m should be minimized. In the UWB receivers, achieving high-order IIP3 is still a challenge because of the wide operation frequency. Based on Fig.1, The output current of the first CDS is given as:

$$\begin{aligned} i_{CDS1} &= i_{dsn} - i_{dsp} \\ &= (g_{n1} + g_{p1})V_i \\ &+ (g_{n1}' - g_{p1}')V_i^2 + (g_{n1}'' + g_{p1}'')V_i^3 \end{aligned} \quad (2)$$

According to Eq. (2), V_{gs} of the secondary CDS is equal to $V_{gs(stage2)} = Z_o i_{CDS1}$, where Z_o is $r_{o3} \parallel r_{o4} \parallel (SC_{gs5})^{-1} \parallel (SC_{gs6})^{-1}$. The output current of the stage2 is similar to Eq. (2) and can be defined based on $V_{gs(stage2)}$ and is given by:

$$\begin{aligned} i_{CDS2} &= i_{dsn} - i_{dsp} \\ &= (g_{n2} + g_{p2})V_{gs} \\ &+ (g_{n2}' - g_{p2}')V_{gs}^2 + (g_{n2}'' + g_{p2}'')V_{gs}^3 \end{aligned} \quad (3)$$

Based on Fig. 2, the output current can be written in terms of CDS stages, CS, and PD as $i_{PD} - i_{path2} + i_{CS}$. An auxiliary transistor is applied as the PD technique for raising the linearity performance at the output node with the current of $i_{PD} = g_{mPD} v_{out} + g'_{mPD} v_{out}^2 + g''_{mPD} v_{out}^3$. Eventually, we represent the output current i_{out} in terms of first, secondary, and thirdly coefficients as:

$$i_{out} = \alpha_1 v_{in} + \alpha_2 v_{in}^2 + \alpha_3 v_{in}^3 \quad (4)$$

Where in Eq. (4), the parameter can be defined according to Eq. (5), Eq. (6), and Eq. (7) as:

$$\alpha_1 = g_{cs} K^{-1} - Z_{o1}(g_{n1} + g_{p1})(g_{n2} + g_{p2}) + g_{mPD} A_V \quad (5)$$

$$\alpha_2 = g_{cs}' K^{-2} - Z_{o1}(g_{n1}' - g_{p1}')(g_{n2} + g_{p2}) - Z_{o1}(g_{n1} + g_{p1})(g_{n2}' - g_{p2}') + g_{mPD}' A_V^{\,2} \quad (6)$$

$$\begin{aligned} \alpha_3 &= g_{cs}'' K^{-3} - Z_{o1}(g_{n1}'' + g_{p1}'')(g_{n2} + g_{p2}) - Z_{o1}(g_{n1} + g_{p1})(g_{n2}' + g_{p2}') \\ &-2Z_{o1}^{\,2}(g_{n1} + g_{p1})(g_{n1}' - g_{p1}')(g_{n2}' - g_{p2}') + g_{mPD}'' A_V^{\,3} \end{aligned} \quad (7)$$

Base on in Eq. (4), α_2 and α_3 are a nonlinear component. The second and third items in Eq. (6) and Eq. (7) are adjustable distortions due to the modified linearizer technique of the second path. IIP3 is defined in Eq. (8) in terms of α_1 and α_3 as:

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \quad (8)$$

Based on Eq. (8) for high-linearity LNA, the expression of α_3 should be minimized. According to Eq. (7), the reduction of the gain leads to improved IIP3. In the proposed structure, the second path is designed for linearity performance, and Eq. (7) confirms this approach by controlling the 2nd and 3rd nonlinear coefficients of the CDS stages.

3.2 Input Matching Network, Noise, and Gain

In the proposed circuit, the LC filter assists in impedance matching progress in the first path to achieve wideband matching. Transistor M_1 is the decisive element of the input stage and L_g and L_s compensate the parasitic capacitance. Considering the transistors connected to the input, such as M_1, M_2 and M_3, the input impedance is derived as:

$$Z_i = \left(\left\{ \left(\frac{L_s g_{m(cs)}}{C_{gs(cs)}} + \frac{1}{SC_{gs(cs)}} + S(L_g + L_s) \right) \middle\| SL_1 \right\} + \frac{1}{SC_1} \right) \middle\| \left(\frac{1}{SC_{gs(n1)}} \right) \middle\| \left(\frac{1}{SC_{gs(p1)}} \right) \quad (9)$$

According to Eq. (9), The active and passive devices used in the first path determine the input impedance, and the second path has a more negligible effect on the input matching. The gain of the proposed LNA can be calculated out as Eq. (10):

$$A_V = Z_{out} \frac{(g_{cs} - KZ_{o1}G_1G_2)}{K(1 - Z_{out}g_{mPD})} \quad (10)$$

Where G_1 and G_2 are $(g_{n1} + g_{p1})$ and $(g_{n2} + g_{p2})$, respectively. K is equal to $S^2(L_g + L_s)C_{gs(sc)} + SL_s g_{m(cs)} + 1$. Amount of Z_{o1} and Z_{OUT} are $(r_{n1} \parallel r_{p1} \parallel (SC_{n2})^{-1} \parallel (SC_{p2})^{-1})$ and $(r_{oPD} \parallel SL_{o2})$, respectively. Reducing the noise of LNA is an attractive part of receiver design. Since the operation frequency of the proposed circuit is above 3GHz, we can ignore the flicker noise. For simplicity, the loading influences of the output resistor are ignored. The noise of biasing resistor is dismissed because of the significant value of the chosen resistor. The NF is calculated by taking a short circuit in the output node and is approximately determined as:

$$NF = 1 + \frac{\overline{|v_{n,out}^2|}}{(A_V)^2} = 1 + \frac{\overline{|i_{n,out}^2|}}{(G_m)^2} \propto \overline{i_{n,out,M_{CS,n1,p1,n2,p2}}^2} \quad (11)$$

The CS transistor plays a considerable component in overall noise performance. In contrast, the noise contribution of other auxiliary transistors is small. So, the output noise current due to M_{cs} and second CDS stage are given by:

$$\overline{i_{nout(CS,n2,p2)}^2} = \frac{4KT\gamma}{\alpha}\{g_{cs} + g_{p2} + g_{n2}\} \left(\frac{r_{on2} \| r_{op2} \| r_{o(cs)} + g_{M2}^{-1}}{r_{on2} \| r_{op2} \| r_{o(cs)}} \right)^2 \quad (12)$$

$$\overline{i_{nout(n1,p1)}^2} = \frac{4KT\gamma}{\alpha}\{g_{p1} + g_{n1}\}^{-1}(G_1G_2Z_{O1})^2 \quad (13)$$

By accurately designing auxiliary transistors, the main transistors' noise will be minimized Fig. 3 shows the noise contribution of essential elements.

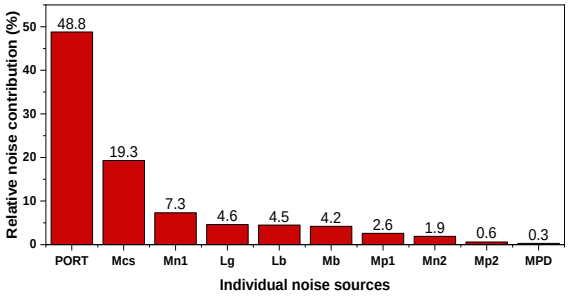

Fig. 3 Noise contribution of important element.

4 Simulation Results and Discussions

To confirm the performance of LNA, the circuit is designed in 180-nm standard CMOS and is simulated by the Cadence Spectre RF. Fig. 4 shows the circuit's layout. The size of the devices is listed in Table. 1. The high IIP3 LNA has a unique superiority in the application where strong jamming signals exist. To this end, using the PD method based on CDS configuration, the average of IIP3 was obtained 8.1 dBm in the whole frequency range, and the IIP3 characteristics of the proposed LNA at different frequency points are plotted in Fig.5. The maximum of the IIP3 is 11.65 dBm, depicted in Fig. 6. A two-tone signal at 5 GHz with 40 MHz separations provides the linearity simulation. The proposed LNA consumes 12.7 mA from a 1.4 V supply voltage.

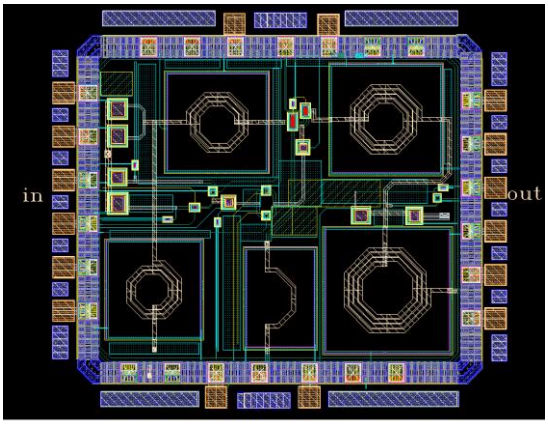

Fig. 4 The layout of the proposed high linear LNA.

Table 1 The value of important devices in UWB-LNA.

device	Size (μm)	device	size
M_{cs}	200	L_q	583 pH
M_{n1}	16	L_s	253 pH
M_{p1}	20	L_b	1.44 nH
M_{n2}	16	M_{PD}	12 µm
M_{p2}	24	M_b	200 µm

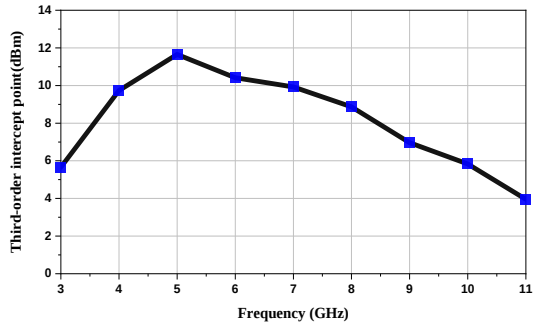

Fig. 5 IIP3 of LNA in the whole frequency band.

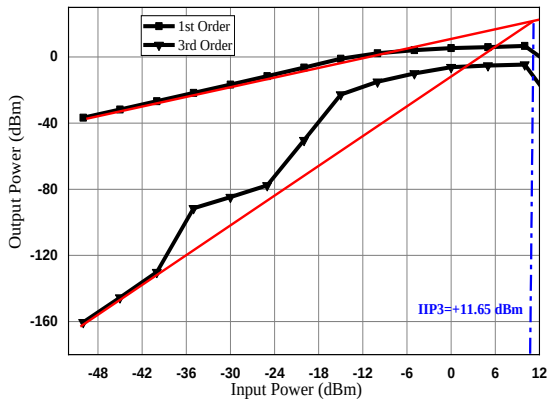

Fig. 6 The linearity of the suggested LNA.

The post-layout simulated results of the S-parameters versus frequency are shown in Fig. 7. S_{11} is lower than -10 in the frequency range of 3.1 to 10.6 GHz. According to Fig. 7, the gain is between 10.08 dB and 13.45 dB over 3.1 to 10.6 GHz. Fig. 8 shows the NF of the proposed LNA versus the frequency. It is below 4 dB at most operating frequencies. To check the stability of the circuit, the parameter of K and $\Delta = S_{22}S_{11} - S_{12}S_{21}$ is drowned in Fig. 9 over the wanted frequency. Stern stability coefficient defined as Eq. (14):

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \quad (14)$$

Fig. 9 shows that K>1 and Δ<1 and the proposed LNA are unconditionally stable.

The proposed structure is investigated under different corners of process, voltage, and temperature (PVT) to confirm the condition of the design. For a change of 10% in supply voltage, the gain and NF were simulated. According to Fig. 10, the circuit has a good response for the lower voltage, but in this case, the amount of IIP3 is degraded, as shown in Fig. 11. The linearity performance is acceptable for all-state because the IIP3 is above -4 dBm in the worst case. In the proposed LNA, the NF and S_{21} versus frequency spectrum from 3 to 11 GHz for different corners and temperatures are investigated as shown in Fig. 12. As it is evident, the highest amount of the NF has occurred in the state of SS and 80 ºC; The range of variations in NF is between 3.6 dB to 5.5 dB. The lowest amount of the NF was obtained in the (FF, - 40ºC) corner, in which variation is between 2.6 dB to 3.8 dB. Post-layout simulation of the IIP3 in different corners at 8GHz is done. Based on the data obtained, in (FF, -40°C) corner, IIP3 is destroyed and (TT, 27°C) corner has minimum variation.

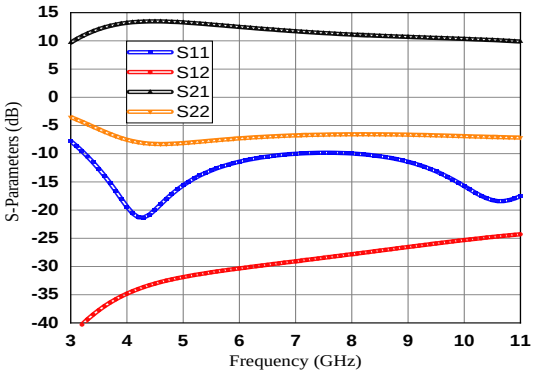

Fig. 7 Post-layout simulated S-parameter at different frequencies.

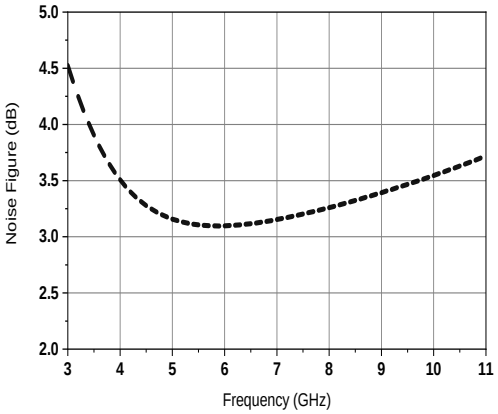

Fig. 8 The noise performance in the total frequency band.

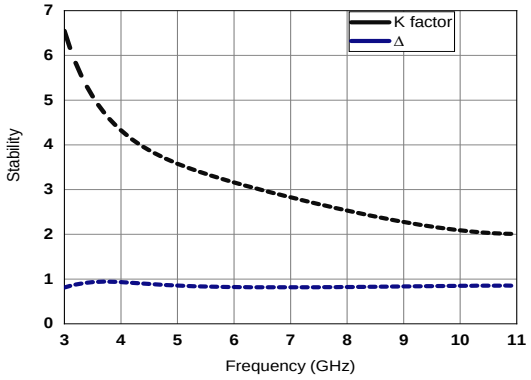

Fig. 9 Simulated stability factor of LNA.

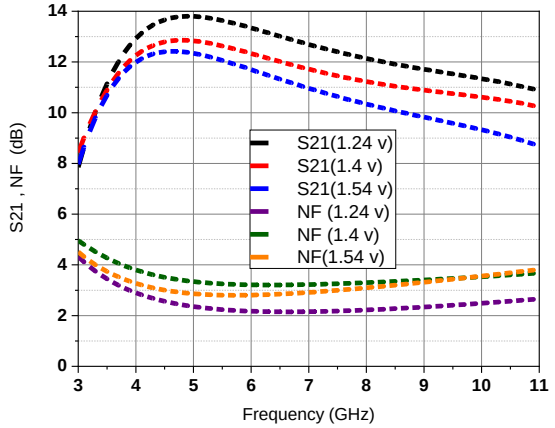

Fig. 10 NF and S_{21} dependence on VDD at varying frequencies.

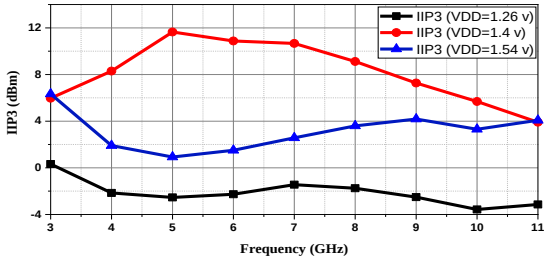

Fig. 11 IIP3 dependence on VDD at varying frequencies.

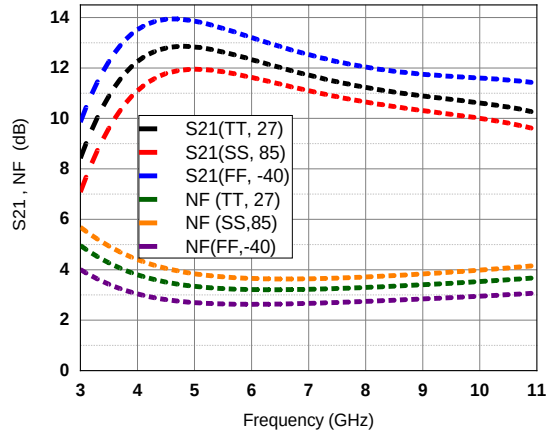

Fig. 12 S_{21} and NF performance at different corner.

Statistical analysis (Monte Carlo) was set to investigate the effect of process and device mismatch. In this work, the statistical behavior of the linearity, gain, and NF was done. Fig. 13 displays the Monte Carlo results for IIP3 base on two tones signal by space frequency of 40 MHz at 5 GHz, representing an IIP3 above 0 dBm. The mean and standard deviation of NF are 3.75 and 0.113 dB, respectively, displayed in Fig. 14. The LNA has mean S_{21} of 12.8 dB with a variation of 0.32 dB, shown in Fig. 15.

The output efficiency of the simulated LNA was summarized in Table 2. Figure-of-merit (FOM) is used to compare the performance between this work and the other published work. The FOM is defined as Eq. (15).

$$FOM = \frac{IIP3_{average}[mW]}{P_{dc}[mW]\times(F_{average}-1)} \times Gain_{average}[abs] \times BW[GHz] \qquad (15)$$

where BW is the bandwidth of the structure. P_{dc} is the power dissipation in mW. $F_{average}$ is the average of the NF. As can be seen in the Table.2, each LNA focuses on one of the output parameters and is designed for a specific application. For example, in the structure of [35], the goal is to improve the gain but, power consumption has increased.

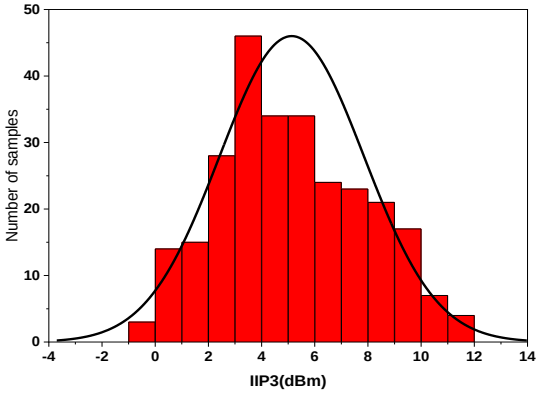

Fig. 13 Monte Carlo simulation for IIP3.

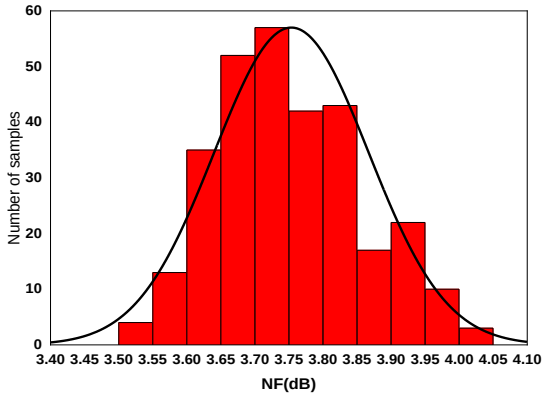

Fig. 14 Monte Carlo simulation for S21.

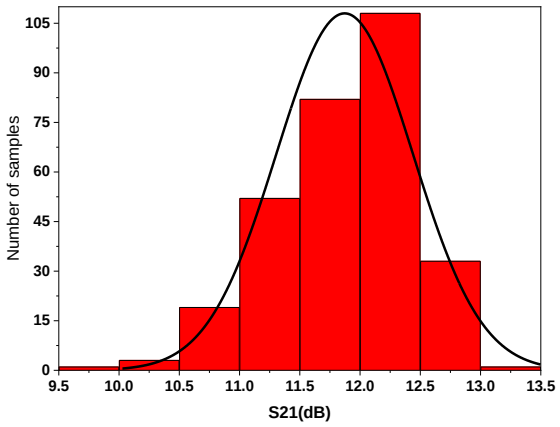

Fig. 15 Monte Carlo simulation for NF.

Table 2 Performance comparison of UWB-LNA with other recently published structures.

References	[31]*	[32]*	[33]**	[34]*	[35]*	[36]**	[37]*	This work*
Tech (nm)	130	130	180	180	180	180	180	180
BW (GHz)	3.1~10.6	3.5~5	3.1~10.6	3~12	3~12	3.1-10.6	0.3~3.5	3.1~10.6
Gain (dB)	11~12.6	10~15	13.2(max)	19.2~20.2	12.75	7-12	14.6	10.08~13.45
NF (dB)	2.9~5.4	3.5~3.9	4.5~6.2	1.72–1.99	4	5.27~7	2.9~3.5	3.1~4.3
S11(dB)	<-10	<-15	<-9.5	<-10	<-10.6	<-10	<-10	<-10
IIP3 (dBm)	-4.6	4	-1.4	-5.5	-3.3	-2.23	1.2~4.7	3.95~11.65
Power(mW)	15.2	21	23	23.23	9.29	4.5	14.8	17.7
FOM	0.55	0.92	0.68	2.21	1.45	1.77	2.49	5.14

*Simulation ** Implementation

In the structure of ref [36], the gain value obtained is similar to the presented paper, but in that structure, the focus was on reducing power consumption, in this article, despite the increase in power consumption compared to that structure, the level of linearity has improved significantly. In present LNA, CDS configuration is the distinguishing feature for enhancing linearity. As seen in Table 2, an acceptable FOM has been obtained compared to recent articles.

5 Conclusion

High linearity diminishes the intermodulation signal and enhances the inviolability of the blocker signal. In the RF front-end UWB receiver, the high linear LNA design has gained considerable interest in modern wireless communications systems. The present LNA covers frequency bands of 3.1 to 10.6 GHz. In the proposed structure, the two-path was defined. The CDS architecture was used in the secondary path to modify the linearity. In the primary path, a source inductive degeneration topology was designed for improving impedance matching. Linearity performance is also improved using the PD method at the output node. Post-layout simulation results of the suggested LNA, designed using 180-nm CMOS technology, present a gain of 11 dB. Also, the average of IIP3 is 8.61 dBm. The LNA consumes 17.7 mW from a 1.4V supply voltage.

Intellectual Property

The authors confirm that they have given due consideration to the protection of intellectual property associated with this work and that there are no impediments to publication, including the timing to publication, with respect to intellectual property.

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Credit Authorship Contribution Statement

B. Dorostkar Yaghouti: Conceptualization, Methodology, Software, Formal analysis, Writing - Original draft, Revise & editing.

Declaration of Competing Interest

The authors hereby confirm that the submitted manuscript is an original work and has not been published so far, is not under consideration for publication by any other journal and will not be submitted to any other journal until the decision will be made by this journal. All authors have approved the manuscript and agree with its submission to "Iranian Journal of Electrical and Electronic Engineering".

Reference

[1] Z. Zhang, Y. Li, K. Mouthaan, and Y. Lian, "A Miniature Mode Reconfigurable Inductorless IR-UWB Transmitter-Receiver for Wireless Short-Range Communication and Vital-Sign Sensing," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 8, Bo. 2, pp. 294-305, 2018.

[2] J. Jiang, J. Kim, A. I. Karsilayan, and J. Silva-Martinez, "A 3-6-GHz Highly Linear I-Channel Receiver with over +3.0-dBm In-Band P1dB and 200-MHz Baseband Bandwidth Suitable for 5G Wireless and Cognitive Radio Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 66, No. 8, pp. 3134-3147, 2019.

[3] C. N. Chen, Y. Chen, Y. Wang, T. Y. Kuo, and H. Wang, "38-GHz CMOS Linearized Receiver with IM3 Suppression, P1 dB/IP3/RR3 Enhancements, and Mitigation of QAM Constellation Diagram Distortion in 5G MMW Systems," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 68, No. 7, pp. 2779-2795, 2020.

[4] K. Wang, Z. Zeng, and J. Sun, "Through-Wall Detection of the Moving Paths and Vital Signs of Human Beings," *IEEE Geoscience and Remote Sensing Letters*, Vol. 16, No. 5, pp. 717–721, 2019.

[5] O. V. Chernoyarov, B. Dobrucky, V. A. Ivanov, and A. N. Faulgaber, "The object detection efficiency in synthetic aperture radar systems," *International Journal of Engineering, Transactions B*, Vol. 33, No. 2, pp. 337-343, 2020.

[6] K. Hari Kishore, V. Senthil Rajan, R. Sanjay, and B. Venkataramani, "Reconfigurable low voltage low power dual-band self-cascode current-reuse quasi-differential LNA for 5G," *Microelectronics Journal*, Vol. 92, 2019.

[7] Y. Ahn, C. Park, J. Lee, and J. Jeong, "A highly linear receiver front-end employing modified derivative superposition method with tuned inductors for 5.25 GHz," *Microelectronics Journal*, Vol. 41, No. 12, pp. 882-888, 2010.

[8] I. Chaharmahali, S. Asadi, B. Dorostkar, M. bosra, and M. Abedini, "A New Method Modifying Single Miller Feedforward Frequency Compensation to Drive Large Capacitive Loads: Putting an Attenuator in the Path," *Analog Integrated Circuits and Signal Processing*, Vol. 93, No. 1, 2017.

[9] M. Mansour, A. Zekry, M. K. Ali, and H. Shawkey, "Integrated Multi-Band RF Transceiver Design for Multi-standard Applications using 130 nm CMOS Technology," *Microelectronics Journal*, p. 105006, 2021.

[10] K. Fazel, "Narrow-band interference rejection in orthogonal multi-carrier spread-spectrum communications," *Annu. Int. Conf. Univers. Pers. Commun. - Rec.*, pp. 46-50, 1994.

[11] B. D. Yaghouti and J. Yavandhasani, "A high linearity UWB LNA using a novel linearizer feedback, based on complementary derivation superposition techniques," *Analog Integrated Circuits and Signal Processing*, Vol. 110, No. 3, pp. 443-454, 2022.

[12] A. P. Tarighat and M. Yargholi, "A CMOS low noise amplifier with employing noise cancellation and modified derivative superposition technique," *Microelectronics Journal*, Vol. 54, pp. 116-125, 2016.

[13] Q. T. Lai and J. F. Mao, "A 0.511 GHz CMOS low noise amplifier using dual-channel shunt technique," *IEEE Microwave and Wireless Components Letters*, Vol. 20, No. 5, pp. 280-282, 2010.

[14] R. Jafarnejad, A. Jannesari, and J. Sobhi, "A sub-2-dB noise figure linear wideband low noise amplifier in 0.18 μm CMOS," *Microelectronics Journal*, Vol. 67, pp. 135-142, 2017.

[15] M. T. Hsu, Y. H. Lin, and Y. Jing-Cheng, "Low power high gain CMOS LNA based on inverter cell and self-body bias for UWB receivers," *Microelectronics Journal*, Vol. 45, No. 11, pp. 1463-1469, 2014.

[16] A. Yarahmadi and A. Jannesari, "Two-path inverter-based low noise amplifier for 10-12 GHz applications," *Microelectronics Journal*, Vol. 50, pp. 76-82, 2016.

[17] T. Chung, H. Lee, D. Jeong, J. Yoon, and B. Kim, "A Wideband CMOS Noise-Canceling Low-Noise Amplifier with High Linearity," *IEEE Microwave and Wireless Components Letters*, Vol. 25, No. 8, pp. 547-549, 2015.

[18] R. Dai, Y. Zheng, J. He, W. Kong, and S. Zou, "A duplex current-reused CMOS LNA with complementary derivative superposition technique," *International Journal of Circuit Theory and Applications*, Vol. 45, No. 1, pp. 110-119, 2017.

[19] F. Daryabari, A. Zahedi, A. Rezaei, and M. Hayati, "Gain-controlled noise-reduction LNA design using source-bulk resistors and double common-source topology," *Integration*, Vol. 68, pp. 50-61, 2019.

[20] B. Guo, J. Chen, L. Li, H. Jin, and G. Yang, "A Wideband Noise-Canceling CMOS LNA with Enhanced Linearity by Using Complementary nMOS and pMOS Configurations," *IEEE Journal of Solid-State Circuits*, Vol. 52, No. 5, pp. 1331-1344, 2017.

[21] B. Guo and X. Li, "A 1.6-9.7 GHz CMOS LNA linearized by post distortion technique," *IEEE Microwave and Wireless Components Letters*, Vol. 23, No. 11, pp. 608-610, 2013.

[22] B. D. Yaghouti and J. Yavandhasani, "A high linearity low power low-noise amplifier designed for ultra-wide-band receivers," *Analog*

Integrated Circuits and Signal Processing, Vol. 107, No. 1, pp. 109-120, 2021.

[23] B. Guo, J. Chen, H. Chen, and X. Wang, "A 0.1-1.4 GHz inductorless low-noise amplifier with 13 dBm IIP3 and 24 dBm IIP2 in 180 nm CMOS," *Modern Physics Letters B*, Vol. 32, No. 2, 2018.

[24] I. Fabiano, M. Ramella, D. Manstretta, and R. Castello, "A +25-dBm IIP3 1.7-2.1-GHz FDD Receiver Front End With Integrated Hybrid Transformer in 28-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 65, No. 11, pp. 4677-4688, 2017.

[25] Y. Y. Tey, H. Ramiah, N. M. Noh, and U. R. Jagadheswaran, "A 50 MHz ~ 10 GHz, 3.3 dB NF, +6 dBm IIP3 resistive feedback common source amplifier for cognitive radio application," *Microelectronics Journal*, Vol. 61, pp. 89-94, 2017.

[26] N. Dehaese, I. Ben Amor, N. Tall, J. Gaubert, R. Vauché, and S. Bourdel, "A self-duty-cycled 7.2–8.5 GHz IR-UWB receiver for low power and low data rate applications," *Analog Integrated Circuits and Signal Processing*, Vol. 92, No. 1, pp. 39-53, 2017.

[27] C. K. Luo, P. S. Gudem, and J. F. Buckwalter, "A 0.4-6-GHz 17-dBm B1dB 36-dBm IIP3 Channel-Selecting Low-Noise Amplifier for SAW-Less 3G/4G FDD Diversity Receivers," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 64, No. 4, pp. 1110-1121, 2016.

[28] B. K. Kim, D. Im, J. Choi, and K. Lee, "A highly linear 1 GHz 1.3 dB NF CMOS low-noise amplifier with complementary transconductance linearization," *IEEE Journal of Solid-State Circuits*, Vol. 49, No. 6, pp. 1286-1302, 2014.

[29] H. Zhang and E. Sánchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: A tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 58, No. 1, pp. 22-36, 2011.

[30] S. Juneja and R. Sharma, "Design of high gain, high reverse isolation and high input matched narrowband lna for gps l1 band applications using 0.18µm technology," *Iranian Journal of Electrical and Electronic Engineering*, Vol. 15, No. 4, pp. 444-452, 2019.

[31] H. Rastegar, S. Saryazdi, and A. Hakimi, "A low power and high linearity UWB low noise amplifier (LNA) for 3.1-10.6 GHz wireless applications in 0.13 µm CMOS process," *Microelectronics Journal*, vol. 44, no. 3, pp. 201–209, 2013.

[32] A. Zokaei and A. Amirabadi, "A 130 nm wideband fully differential linear low noise amplifier," *Microelectronics Journal*, Vol. 46, No. 9, pp. 825-833, 2015.

[33] B. Park, S. Choi, and S. Hong, "A low-noise amplifier with tunable interference rejection for 3.1- to 10.6-GHz UWB systems," *IEEE Microwave and Wireless Components Letters*, Vol. 20, No. 1, pp. 40-42, 2010.

[34] M. Hayati, S. Cheraghaliei, and S. Zarghami, "Design of UWB low noise amplifier using noise-canceling and current-reused techniques," *Integration*, Vol. 60, pp. 232-239, 2018.

[35] M. Babasafari and M. Yargholi, "A Low Power CMOS UWB LNA with Dual-band Notch Filter Using Forward Body Biasing," *IETE Journal of Research.*, Vol. 66, No. 2, pp. 127-138, 2020.

[36] R. M. Weng, C. Y. Liu, and P. C. Lin, "A low-power full-band low-noise amplifier for ultra-wideband receivers," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 58, No. 8, pp. 2077-2083, 2010.

[37] D. Huang, X. Yang, H. Chen, M. I. Khan, and F. Lin, "A 0.3–3.5 GHz active-feedback low-noise amplifier with linearization design for wideband receivers," *AEU-International Journal of Electronics and Communications*, Vol. 84, pp. 192-198, 2018.

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