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Proposing Very Low Power Three-Valued Flip-Flops by Using CNTFET Transistors

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Abstract: The scaling limitations of Complementary Metal-Oxide-Semiconductor (CMOS) transistors to achieve better performance have led to the attention of other structures to improve circuit performance. One of these structures is multi-valued circuits. In this paper, we will first study Carbon Nanotube Transistors (CNT). CNT transistors offer a viable means to implement multi-valued logic due to their variable and controllable threshold voltage. Subsequently, we delve into the realm of three-valued flip-flop circuits, which find extensive utility in digital electronics. Leveraging the insights gained from our analysis, we propose a novel D-type flip-flop structure. The presented structure boasts a remarkably low power consumption, showcasing a reduction exceeding 61% compared to other existing structures. Furthermore, the proposed circuit incorporates a reduced number of transistors, resulting in a reduced footprint. Importantly, this circuit exhibits negligible static power consumption in generating intermediate values, rendering it robust against process variations. Overall, the proposed circuits demonstrate a 29.7% increase in delay compared to the compared structures. However, they showcase a 96.1% reduction in power-delay product (PDP) compared to the other structures. The number of transistors is also 8.3% less than other structures. Additionally, their figure of merits (FOM) are 19.7% better than the best-compared circuit, underscoring its advantages in power efficiency, chip area, and performance.

Keywords: CNTFET, Flip-Flop, High Performance, Low Power, Multi-Valued.

1 Introduction

A large part of the success of the CMOS transistor is due to its scalability to much smaller dimensions, which results in better performance. This trend continues by Moore's law, and silicon-based technology has grown significantly over the past few decades [1]. However, as the size of MOSFET transistors approaches their limits in the nanometer region, the semiconductor industry is looking for alternative materials and components to integrate with, and eventually likely replace current silicon-based technology. During the past few decades, Carbon Nanotubes (CNTs) have attracted much attention in the field of electronics due to their unique structure and excellent physical properties [2-9]. The use of CNTs in the channel region of the FET in a laboratory rather than a commercial manner to obtain a new device called the Carbon Nanotube Field Effect Transistor (CNTFET) was first demonstrated in 1998 [10]. Due to the high electrical mobility, high ballistic transmission, and mechanical and thermal stability of CNT, CNTFETs are considered as one of the promising candidates for post-silicon electronics [11-14].

Paper [15] has given a complete review of CNTFET. In [15], the fabrication of CNTs as well as CNTFETs, methods of obtaining specific types of CNTs, their purification (choice of suitable nanotubes), and proper placement of CNTs are discussed. According to the current trend of widespread interest in CNTFETs, in the near future, suitable CNTs in terms of dimensions and structure may be placed in the channel region with very few changes to provide the conditions for their

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commercialization. Although research related to CNT fabrication and polish issues is still ongoing, we can explore the possibility of creating new circuits using CNTFETs for high-performance implementations [3], [5].

Today, many studies continue to design and investigate the use of CNTFETs in logic gates and evaluate their performance compared to existing CMOS technology. CNTFET circuit applications include binary logic gates [7], [16-19], three-valued logic gates [6], three-valued and binary memory cells [8], [18], and multi-valued logic [9], [20]. The use of CNTFETs for multi-valued logic is of great interest because the threshold voltage of CNTFETs can be controlled by the appropriate selection of the CNT crystal vector. The crystal vector of graphite networks determines their physical structure. Logical circuits, including adders, multipliers, as well as various memories, have been designed using CNTFET to obtain lower latency, reduce power consumption, and reduce the complexity of connections and interconnections of the chip.

Currently, the interconnections of the chip have become a serious challenge due to the use of many modules in one chip. In a typical binary circuit chip, 70% of the area is occupied by interconnections, 20% by insulation, and only 10% by transistors [21]. Also, these connections waste a lot of power, increase the delay time, and cause destructive and unwanted connection effects such as increasing capacitors, resistors, and inductors. Multi-Valued Logic (MVL) can solve and improve the routing problems of binary system VLSI circuits. In multi-valued mode, fewer numbers are required to store, display, and calculate data. Its other advantages are high calculation speed, memories with high storage density, the ability to send and receive high data, and the simplicity of checking and testing it. However, the MVL system has a higher signal level than the binary system. This phenomenon and the noise of the system signal, which is the noise margin, are more vulnerable to unwanted manufacturing changes. If this problem is not solved properly, MVL circuits can no longer be used to design electronic systems, because due to the sensitivity of intermediate values to noise, their values will change unintentionally and the results will be wrong.

In this paper, we initially investigated multi-valued D flip-flop (DFF) circuits and assessed their advantages and disadvantages. One of the primary challenges associated with these circuits is the presence of static power consumption required to produce the intermediate value. By introducing a novel circuit design, we addressed this issue and successfully reduced the circuit's power consumption. Furthermore, the proposed circuit features a decreased number of transistors compared to competing designs, leading to a minimized on-chip footprint.

2 Multi-Valued Logic and CNTFET

Unlike conventional binary digital arithmetic, MVL uses more than two logic states. Today, three-valued logic has attracted considerable attention for the design of digital systems due to its potential advantages over binary logic. The advantages of MVL are the simplicity and efficiency of the design, the need for less memory and fewer connections, the reduction of the chip area, the bandwidth of parallel and serial transmission, the high potential for increasing the speed of calculations, reducing the switching activity, and implementing many mathematical and logical functions in one chip unit are some of them [6], [8, 9]. The structure of the CNTFET is similar to the conventional MOSFET in that a single-walled CNT semiconductor is used in the channel region. The suitability of the CNTFET for application in three-valued logic lies in the fact that the threshold voltage (V_{th}) of the CNTFET can be controlled by a suitable choice of the chiral vector of the CNT. This is due to the dependence of the threshold voltage for a CNTFET on the band gap of the CNT, which is related to the orientation of the graphene to obtain the CNT. In general, the chiral vector for a particular CNT is represented by two integers (n, m) [22]. In addition, the diameter of a CNT in terms of (n, m) is as follows [22]:

$$d_{CNT} = \frac{a}{\pi}(n^2 + m^2 + nm)^{1/2}$$
$$a = |\overrightarrow{a_1}| = |\overrightarrow{a_2}| = 1.42 \times \sqrt{3} = 2.46A^o \quad (1)$$

where a_1 and a_2 are the initial vectors of graphene.

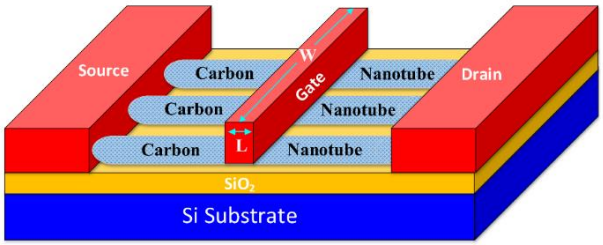

Fig. 1 The structure of a CNTFET that uses several nanotubes in the channel region [9].

The structure of a CNTFET is shown in Fig. 1. In this form, doped-free semiconductor nanotubes are placed under the gate as the channel region, while heavily doped CNT segments are placed between the gate and drain/source to provide lower on-state resistance. When the gate potential increases, the device is electrostatically turned on or off through the gate, and the threshold voltage of the internal CNT in the channel, which is an inverse function of the diameter size, is given by [22]:

$$V_{th} = \frac{aV_\pi}{\sqrt{3}ed_{CNT}} \quad (2)$$

where, V_π = 3.033 eV is the bond energy of carbon in

the tight-binding model, *e* is the electron charge unit, and d_{CNT} is the diameter of the CNT used in the channel. It is obvious from Eq. (2) that the threshold voltage of CNTFET changes with the diameter of CNT in the opposite direction, and in this way, the required value can be reached by choosing an appropriate chiral vector. This is the major advantage of CNTFETs for use in three-valued logic.

The Current-Voltage (*I*-*V*) diagram of CNTFET with different gate-source voltage (V_{gs}) is shown Fig. 2. This figure shows that the diagram of CNTFET is similar to MOSFET. Due to the possibility of different threshold voltage and MOSFET characteristics such as (*I*-*V*), CNTFET is suitable for implementing three-valued logic.

3 Review of Works

Latch and flip-flop are basic components that play a vital role in determining the performance of sequential circuit designs. Some of the most common digital applications where flip-flop designs are used are data storage, frequency dividers, registers and counters, etc. [23]-[25]. Multi-valued logic design provides the possibility of increasing computational capability in sequential logic designs. For example, consider a case of designing a 25-digit counter circuit. If a typical binary logic design is used, 5 flip-flops are required for the implementation. On the other hand, if three-valued logic is used to implement a 25-bit counter, 3 flip-flops are sufficient to implement a given number of states. Also, the need for clock resources is reduced because fewer flip-flops are required for implementation. It is a well-known fact that one of the dominant sources of overhead in electronic sequential designs is due to the regular transition of clock inputs [1]. Therefore, by using a three-valued logic design, the power efficiency of the designs can also be improved due to the reduction in the number of clock inputs applied across the flip-flops. Therefore, by exploiting the design of three-valued logic in latch and flip-flop structures, it is possible to increase the number of states with less hardware requirements, which leads to a reduction in the complexity of the connection for digital designs [24].

Therefore, in this paper, three-valued flip-flop cells are designed using an efficient voltage divider topology, which in turn provides less circuit complexity along with higher energy efficiency.

Three-valued logic inserts a third value into the Boolean space of binary logic. In three-valued logic, operations are performed at 3 different logic levels called logic 0, 1, and 2, which in turn correspond to voltage levels 0, $V_{dd}/2$, and V_{dd}. The next section has discussed the three-valued logic implementation of D-flip-flop designs using CNTFETs.

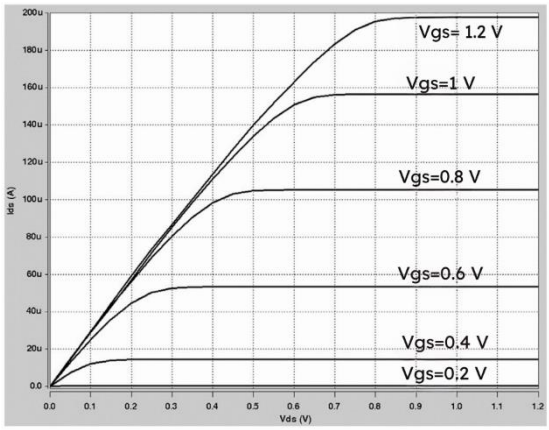

Fig. 2 Current-voltage diagram of N-type CNT transistor at different gate-source voltages.

3.1 Three-Valued Logic

The various three-valued logic families are available for designing three-valued logic gates [20]. The resulting design performance depends on the efficiency of the voltage divider topology adopted to realize the intermediate logic level ($V_{dd}/2$). Initially, Lin et al. [26] presented the STI scheme that used P-CNTFET active load or diode-connected load transistors instead of resistive load in realizing the voltage divider network. The design of [26] provides better performance in terms of PDP efficiency and chip area. Another method defined in [27] for the design of three-valued logic gates is to take the arithmetic mean of the negative and positive complements to calculate the standard output function. In the STI design [27], NTI and PTI equivalents are first generated and then transferred to P- and N-type transistors to obtain the final three-valued outputs. The design [27] offers the advantages of better drive capability with a lower overhead level but has the problem of high static power dissipation compared to previous designs. In the realization of STI using transistor load topology [28], the design [27] always replaces P-type and N-type transistors for voltage division with the gate transistor connected to the source terminal. The last work of Tabrizchi et al. [29] presents another efficient three-valued logic family. In the STI design structure [29], the voltage divider section has been redesigned where the position of the top and bottom grid transistors that used to generate the intermediate logic using voltage division has been changed and current division has been used instead.

3.2 Three-Valued Flip-Flop

In sequential logic design, latch and flip-flop designs are the basic elements used for data storage. A bit of data can be stored in a latch or a flip-flop. A latch is a level-sensitive gate where the output is affected by the input logic level rather than the rising or falling edge of the applied clock signal. In the normal flip-flop design, two

latches are used as master and slave, one is sensitive to high level and the other is sensitive to low level. In the implementation of a three-valued flip-flop, the change of the level 0 of the clock signal to the value of 2 is a rising edge, which should transfer the input D value to the output Q. So there is no intermediate level in the clock signal. The performance table of D-type flip-flops is given in Table 1.

Table 1 Three-value D-type flip-flop operation

Clock	D (input)	Q (output)
0 to 2	0	X to 0
0 to 2	1	X to 1
0 to 2	2	X to 2

In [30], a three-value D-type flip-flop is presented, which is shown in Fig. 3. This structure consists of two parts, Master and Slave. Both parts are level-sensitive, and their composition is edge-sensitive. This structure has good stability to changes in input noise, construction tools, and power sources [30]. The main problem of this structure is its very high-power consumption, which is due to the large number of transistors, which is 40. The delay value stated in the article obtained from the simulation is equal to 23.5 ps, which is the delay of the slave input to its output. The delay value of the Master input to the Slave input has not been calculated. Due to the similar structure of Slave and Master, their delay will be almost the same. So, the total circuit delay is equal to 47 ps. Because the circuit frequency is higher than this value, the circuit will not work properly.

Another advantage of the structure presented in [30] is the presence of Q+ output, which is equal to Q+1. The existence of this output is very efficient for the implementation of the three-valued counter, which is also mentioned in the article, and a new counter structure is also proposed using the presented flip-flop.

In reference [36], a D-type flip-flop that is master and slave is presented. This circuit is given in Fig. 4. This circuit has a smaller number of transistors than the other circuits presented. Also, the delay value of this structure is very good and it has the ability to drive the output well. This circuit drives the values 2 and 0 well, but in the transfer mode, it has a static power intermediate value, which causes the total power consumption to increase in addition to reducing the drive power.

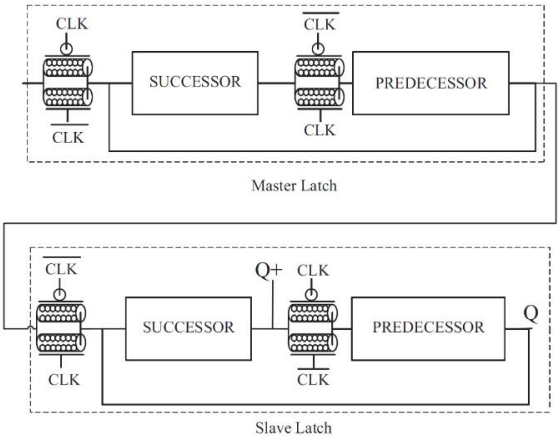

Fig. 3 The structure presented for D-type flip-flop in the article [30], which consists of two latches, Master and Slave.

In [33], a three-valued flip-flop circuit based on CNTFET transistors is presented. In this circuit, three-value structure basic gates are used. This structure will have a high delay due to the use of basic gates and not optimizing the structure of both power consumption.

In [37], a new D-type flip-flop is presented with two latches. Additionally, a multiplexer is employed for the design. While this structure yields good power efficiency, its delay in series circuits drops significantly. To address the issue, the inclusion of a buffer between blocks is recommended, albeit this may lead to an increase in circuit delay. Similarly, in [38], a new structure based on multiplexer is proposed, similar to [37]. However, this structure faces the challenge of reducing the output driving power in series circuits. It's worth noting that the proposed circuits in [37] and [38] lack the presence of the RESET and SET signals.

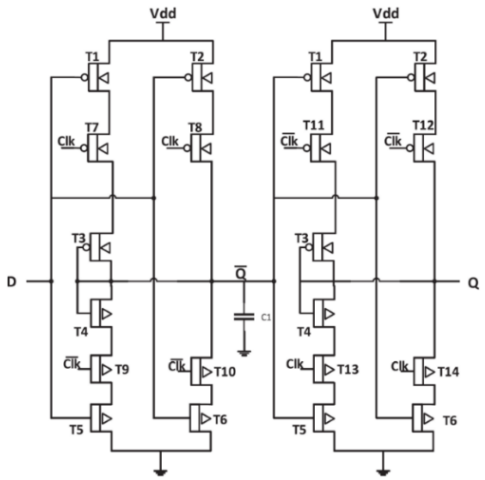

Fig. 4 Three-valued flip-flop structure presented in [36].

In the article [31], a new flip-flop structure using pulse generation is presented (Fig. 5 and Fig. 6). This structure has fewer transistors than [30]. Also, two signals S and R

have been implemented in this structure. The only problem with this structure is its high-power consumption due to the presence of static current in the output during intermediate value generation. This static current also greatly reduces the output drive power.

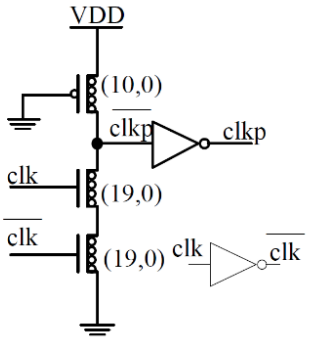

Fig. 5 PG pulse generator circuit [31] (The numbers in parentheses (*n, m*) represent the chiral vector for the CNTs).

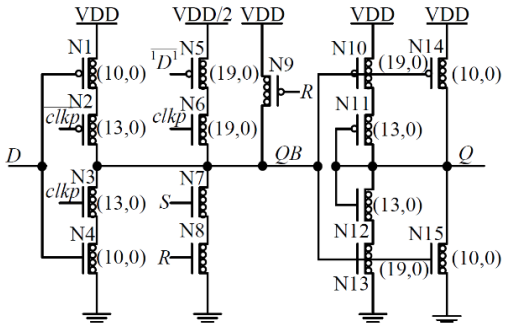

Fig. 6 Flip-flop structure presented in [31].

4 The Proposed Circuits and Simulation Results

The circuit presented in [31] should have a low power consumption due to the low transistor count, but due to the high static power consumption, this has not been achieved. In the following, we will try to solve the problem by proposing new circuits.

4.1 The First Proposed Circuit

The first proposed circuit is shown in Fig. 7. In this circuit, by removing the static power at the state when the output is equal to 1, the total power consumption has been greatly reduced. Also, by solving this problem, the circuit has become more resistant to manufacturing variations because the structure shown in Fig. 6 will not produce a correct value for '1' for changing one of the transistors connected to the output Q, and logic '1' will be unavailable. But in the first proposed circuit, this problem is solved and the circuit is very invulnerable.

In most of the compared circuits, a structure is used to produce the intermediate value ($V_{dd}/2$), where the short-circuit static current is continuously drawn from the power supply. This greatly increases the power consumption and reduces the output driveability. In the proposed circuit, we provided another structure for producing the intermediate value. When the output is in the '1' state, i.e., $V_{dd}/2$, the pull-down transistor N11 disconnects the direct path between supply voltages and ground, eliminating short-circuit static power dissipation.

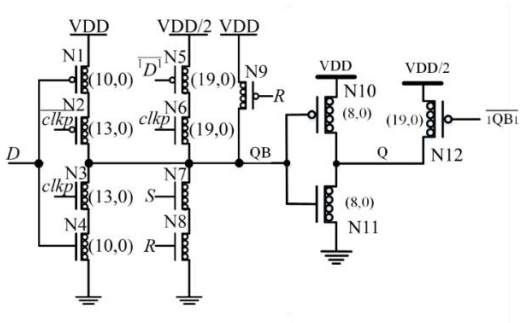

Fig. 7 The first proposed circuit for a multi-valued CNTFET flip-flop circuit.

In the proposed circuit, there is no static power consumption caused by the current between the power supply and ground. Also, the presented circuit has much better drive power than the previous circuit. The final voltages are also very accurate and are exactly equal to the power source voltage. In multi-value circuits, due to the presence of static currents, the power consumption usually increases a lot. In the proposed circuit, this current is completely removed. Also, this circuit has the ability to drive the output so that the final output voltage does not change. That is, if a static current is drawn in a circuit from the input, the proposed circuit will have the ability to drive it without changing the output voltage level. Of course, the provided circuit has both Reset and Set input signals, and if they are not needed, the circuit will be much simpler and the speed and power consumption will be reduced.

4.2 The Second Proposed Circuit

In the first proposed circuit, by removing the static power consumption at input 1, the total power consumption has been significantly reduced. However, the amount of critical circuit delay has also increased, which is not favorable for high-speed applications. The critical delay of the first proposed circuit is in input mode 1, which can be reduced by adding a charging circuit and improving the overall delay of the circuit. The second proposed circuit is shown in the Fig. 8.

4.3 Simulations and Results

To simulate the circuits, Synopsys HSPICE software is used in the 32 nm CNTFET technology presented in [32]. The voltage of the power supply is equal to 0.9 volts.

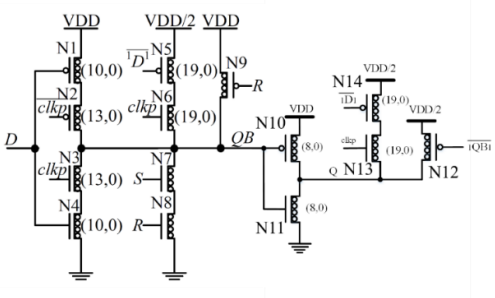

Fig. 8 Second proposed circuit for three-valued flip-flop in CNTFET structure.

The input frequency of the clock signal is equal to 250 MHz. The delay value is calculated from 50% of input to 50% of output and the power consumption is the average power consumption. The output obtained from the circuit simulation is given in Fig. 9.

Table 2 shows the values obtained from the simulation of three-valued flip-flop circuits at a voltage of 0.9 V and a working frequency of 250 MHz. As it is clear from Table 2, the results of the second proposed circuit are better than the rest of the compared circuits. It has very low power consumption. The second proposed circuit has a much better PDP than the compared circuits (10% improved compared to the best circuit [35]), which is due to reducing the power consumption of the circuit. The proposed circuit consumes very little power and does not consume any static power due to the elimination of short circuit power in the intermediate state. The second proposed circuit has a very good condition in terms of delay and can be used in high-speed applications.

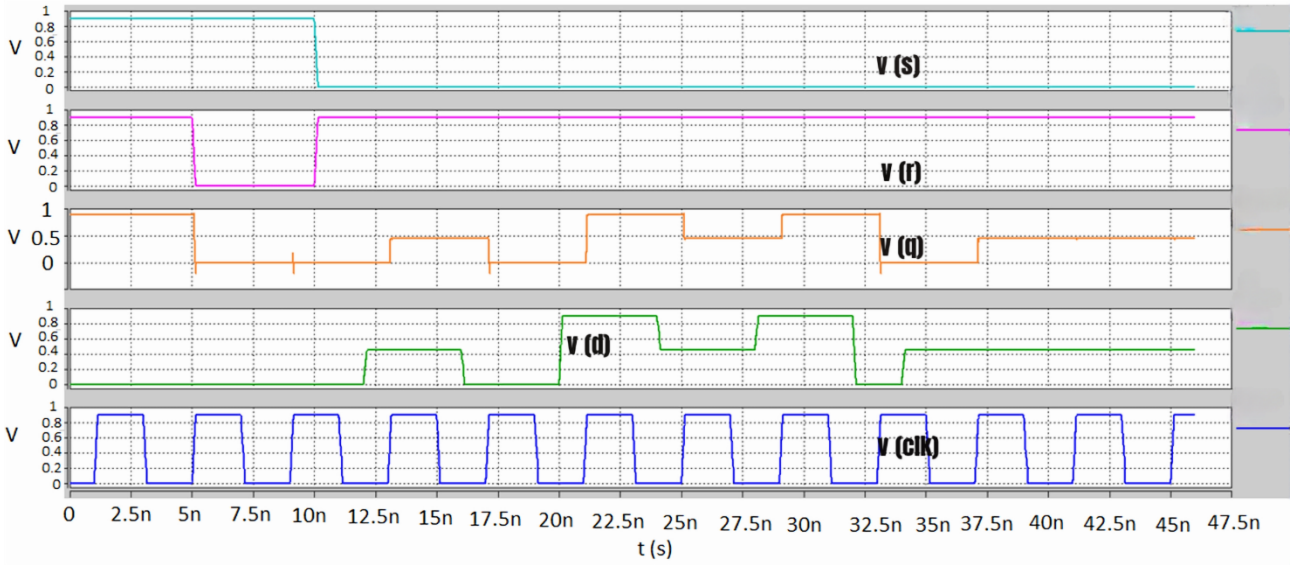

Fig. 9 Overall simulation output of the second proposed circuit for three-valued flip-flop based on CNTFET transistors.

Table 2 Comparison of the results obtained from the simulation of three-valued flip-flop circuits

Design	Power (nW)	Delay (pS)	PDP (aJ)	# Trans	FOM (PDP × #Trans)
[30]	178	23.5(47)	4.18(8.37)	40	167.2(334.8)
[36]	8600	86.6	744.7	14	10425.8
[33]	471	44.1	20.77	46	955.42
[31]	200.8	45.6	9.16	26	238.16
[34]	1290	35	45.15	40	1806
[37]	135	90.1	12.1	40	484
[38]	327	28.6	9.35	22	205.7
First Proposed	69.3	74.7	5.18	29	150.22
Second Proposed	72.5	52.7	3.82	31	118.42

The best delay is related to circuit [35], which of course is due to not considering the delay of the master section. The paper [36] is very optimal in terms of the number of transistors used, but due to its high static power, it consumes a lot of energy. Since the proposed structure does not have the best delay and transistor count, a figure of merit (FOM) has been defined as the product of power, delay, and the number of transistors. The results are presented in Table 2 for various structures. As observed, the proposed structures have the best FOM, indicating the best compromise among these parameters compared to other structures.

Figures 10, 11, and 12 show the results obtained for simulating the circuits, taking into account the changes in the manufacturing process assuming variations of 5%, 10%, and 15% in channel length and oxide thickness. As can be seen, the proposed circuits have shown very good resilience to process variations.

In Fig. 13, 14, and 15, the proposed circuits have been examined in terms of working temperature changes. As can be seen, the proposed circuits have a much better performance than the circuit [31].

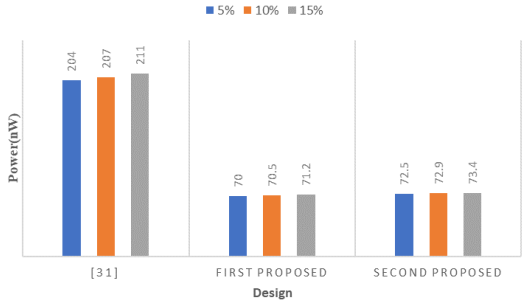

Fig. 10 Monte Carlo simulation results of power versus variations for three-valued flip-flop.

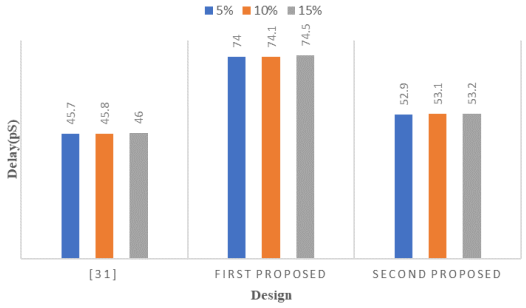

Fig. 11 Monte Carlo simulation results of delay versus variations for three-valued flip-flop.

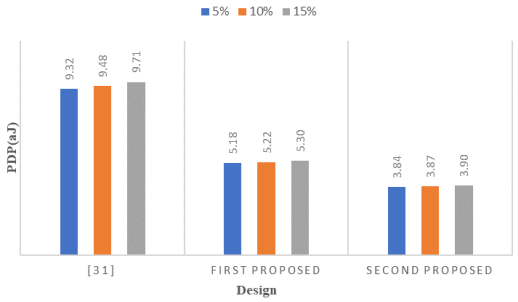

Fig. 12 Monte Carlo simulation results of PDP versus variations for three-valued flip-flop.

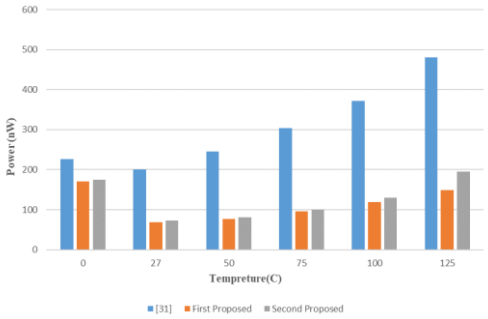

Fig. 13 Power consumption of three-valued flip-flop according to temperature changes.

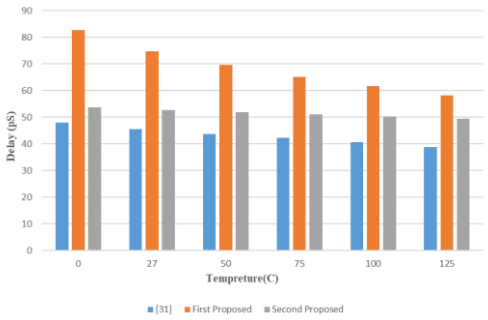

Fig. 14 Three-valued flip-flop delay in terms of temperature changes.

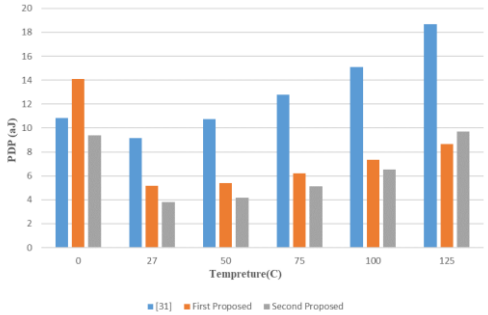

Fig. 15 The PDP value of the three-valued flip-flop in terms of temperature changes.

5 Conclusion

In this paper, we first evaluated the CNT transistor. Then, we explored three-valued flip-flop circuits and by eliminating the static power consumption of one of the structures, we proposed a new circuit for three-valued flip-flops. This proposed structure has the lowest amount of power consumption compared to other structures. Also, the presented circuit has the lowest value in terms of PDP and is very optimal in terms of the number of transistors used. The proposed structure also has two input signals S and R, which are required for implementation as registers and counters.

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