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Carbon Nanotube Based Variation Tolerant Low Power Cache Memory for 5G Networks

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Abstract: The overall performance of any integrated circuit is defined by its proper memory design, as it is a mandatory and major block which requires more area and power. The prime interest of this article is to design a memory structure which is tolerant to variations in CNFET (Carbon nanotube field effect transistor) parameters like pitch, diameter and number of CNT tubes, and also offer low power and high speed of operation. In this context, CNFET based stacked SRAM (Static random access memory) design is proposed to attain the above mentioned criteria. Concept of stack effect is utilized in the cross coupled inverter section of the memory structure to attain low power. The power, speed and energy analysis for the proposed structure is done, and compared with the conventional structures to justify the proposed memory cell performance. HSPICE simulation results has confirmed that the proposed structure offers about 34%, 54% and 95% power saving in hold mode, read mode and write mode respectively. In speed and energy point of view it provides about 97% read delay, 92% write delay and 98% energy savings than the conventional memory structures. These results make it clear that the proposed SRAM is suitable for the 5G networks where circuit speed, power and energy consumption are the major concern.

Keywords: Carbon nanotube (CNT), CNFET, SRAM, Low power, VLSI, 5G networks.

1 Introduction and Motivation

VERY large scale integration (VLSI) forms the basis in all the emerging and advanced hardware systems like 5G networks, wearable health assist devices, bio medical applications, Internet of Things (IoT), embedded systems, signal processing systems etc. For instance in high performance applications like 5G networks, high data rate, decreased latency, good quality of service and increased capacity are the prime objectives. Drastic improvements are required in the VLSI chip design to meet out these demands [1-2]. The memory section dominates the major chip area, and hence proper SRAM design has become the ultimate concern in VLSI design.

With accordance to growing technology, SRAM cell size has been scaled and reached a level where further scaling will affect its performance due to process induced variations and threshold voltage variability of MOSFETs [3]. Also MOSFET based circuits suffer from high leakage power: power consumed by an integrated circuit in idle state. Therefore, alternatives like CNFET based memory designs has gained importance in nanoscale regime, due to its better properties compared to MOSFETs, and it will play a major role in future IC industry [4]. Since the V-I characteristics are nearly same as that of the V-I MOSFETs, CNFETS can be extended to electronic circuits designed using MOSFETs. The basic structure of CNFET is shown in Fig.1 and its performance depends on the device parameters like threshold voltage, number of CNT tubes (N), pitch, CNT diameter, oxide thickness etc. [6-9].

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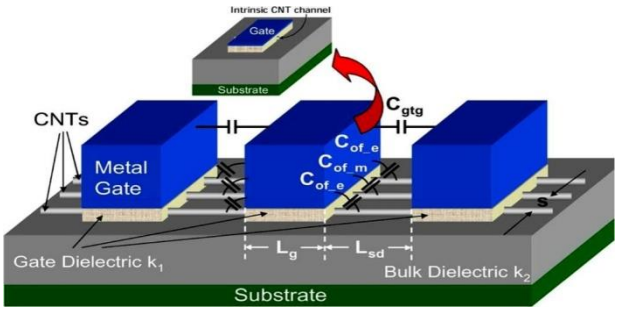

Fig. 1 CNFET structure [5]

Extensive research has been carried out with respect to memory cell design and lot of literature is found especially in SRAM design. Conventional random access memory structure has six transistors (6T SRAM). It has two cross coupled inverters for storing the one bit data, and two access transistors to enable access to the storage nodes [10]. Power consumed in 6T SRAM is high and its noise margin is low. C8TRB (Conventional 8T Read Buffer) SRAM structure shown in Fig.2 improves the stability compared to 6T SRAM, by adding a read buffer (M7 and M8) [11].The read buffer decouples the read path from the storage nodes, leading to high read stability but it consumes more power. 4N4P-PRD SRAM is a modified version of C8TRB SRAM where the N-type transistors in the read buffer are replaced with P-type transistors. Driver P-type transistors are optimized with four tubes and read buffer transistors with six tubes. The N-type access transistors are optimized with six tubes and cross coupled transistors with four tubes in 4N4P-PRD SRAM [12]. High read speed is attained by optimizing the number of tubes in each transistor but the area requirement is more.

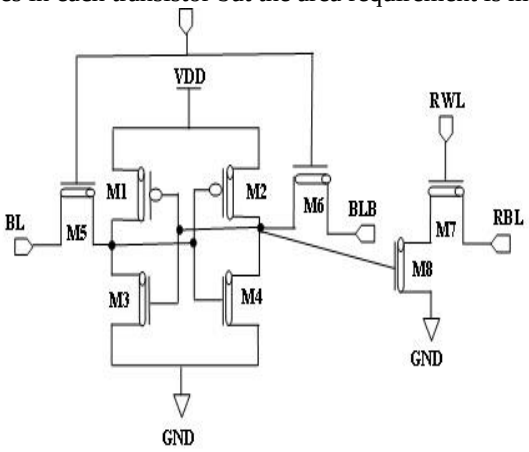

Fig.2 C8TRB SRAM [11]

Fine grain bit line stacked 8T SRAM minimizes leakage current by utilizing word line driver power gating, which also aids to reduce the power [13]. Single ended read port 8T memory cell provides immunity against read upset and improves the read margin of the cell. For this an inverter is used between the storage node and read line to improve the SNM [14]. 8T read decoupled dual port memory with dual threshold transistors minimizes the power consumption and maximizes the speed, where cross coupled inverters are optimized as high threshold transistors and access transistors as low threshold transistors [15]. Area is increased because of dual port usage. C7TRB SRAM shown in Fig.3 also has separate read buffer (M6 and M7), but during the write operation, if QB is '1', both M6 and M7 will be partially '*on*' leading to more power consumption and delay [16]. In this paper, a stacked CNFET SRAM memory structure is proposed and investigated for high speed, low power and low energy. The manuscript is organized as: Section 2 presents the proposed memory structure and its different modes of operation. Also the concept of stacking and its contribution in minimizing power is provided. Section 3 deals with the simulation results and its analysis to establish the stacked memory performs better than conventional structures. Section 4 concludes the work.

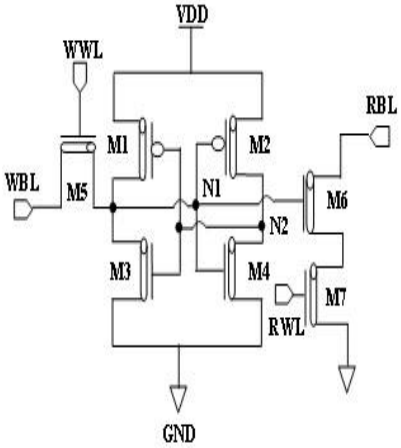

Fig. 3 C7TRB SRAM [16]

2 Proposed Memory Structure

The proposed eight transistor stacked SRAM (P8TS SRAM) structure for enhancing the circuit speed as well as for minimizing power in standby and active mode is presented in Fig.4. Transistors M3 and M4 are the access transistors whose switching operation is managed by the word line (WL). The cross coupled inverters store the data and the nodes Q and QB are termed as the storage nodes. In order to attain low power circuit design, stacking is done in the design of the proposed memory structure. The N-type CNFET transistors M5 and M6 form one set of stacked pair while M7 and M8 form another set of stacked transistors. Thus, the cross coupled inverters in P8TS SRAM have six transistors which aids to alleviate power.

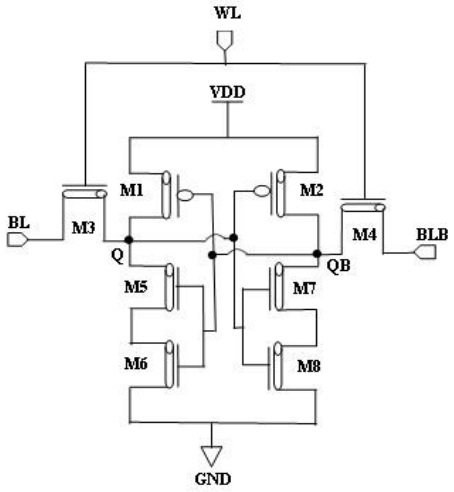

Fig. 4 Proposed P8TS SRAM structure

Importance of stacking effect or self-reverse bias is that the currents passing through stacked transistors decrease when more than one transistor is '*off*' thereby minimizing the power.

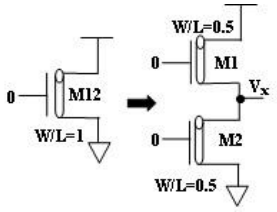

Fig. 5 Forced stack effect

Effect of stack effect on current can be proved by the Eq. (1) to Eq. (5). The leakage current of a MOS transistor is given by Eq. (1) by the assumption that *Vds*>50mV.

$$I_{leakM12} = I_{off} 10^{\frac{V_{GS}+\eta(V_{DS}-V_{DD})-K_\gamma V_{SB}}{S}} \quad (1)$$

where I_{off} - sub threshold current when V_{GS}=0 and V_{DS}=$V_{DD,}$ S- sub threshold slope, η- DIBL coefficient and $K\gamma$ - body effect coefficient. From figure 5, for transistor M1, V_{GS} = -V_X, V_{DS}= V_{DD}-V_X, V_{SB}=V_X. Similarly for transistor M2, V_{GS} = *0*, V_{DS}=V_X , V_{SB}=*0*. Referring Eq.1, the leakage of stacked transistors shown in Fig.5 can be written as

$$I_{leakM1} = I_{off} 10^{\frac{-V_x+\eta\left((V_{DD}-V_x)-V_{DD}\right)-K_\gamma V_x}{S}} \quad (2)$$

$$I_{leakM2} = I_{off} 10^{\frac{\eta(V_x-V_{DD})}{S}} \quad (3)$$

where V_x is the intermediate voltage at which the current of the transistors M1 and M2 in the stacked pair is same. Hence the expression for V_x is obtained by equating I_{leakMI}=I_{leakM2} and is given in Eq.4.

$$V_x = \frac{\eta V_{DD}}{1+2\eta+K_\gamma} \quad (4)$$

Eq. 5 represents the total stacked pair current which is determined by substituting V_x in either Eq. (2) or Eq.(3).

$$I_{stack} \approx I_{off} 10^{\frac{-\eta V_{DD}}{S}} \quad (5)$$

Using standard values (for a 65 nm MOS transistor, S=about 100 mV/decade, η=100 mV/V, V_{DD}=1 V) in Eq.(5), I_{stack}/I_{off} =0.1. Therefore it is obvious that the stacked pair minimizes leakage by a factor of about 10. The I_{off} currents per gate capacitance of N-MOSFET and N-CNFET are made equal, if the effective gate capacitance value is 1.1fF/μm and 3.6aF/FET respectively. For the same values, I_{off} currents per gate capacitance of P-MOSFET and P-CNFET are also equal [17]. Considering this equivalence, Eq. (1) to Eq. (5) is applicable to CNFETs also, proving the stacking effect has considerable effect in CNFET circuit designs too.

2.1 Hold State

Fig.6 shows the proposed P8TS SRAM in hold mode wherein the WL control signal is made zero. The access transistors are '*off*' in this mode and the cross coupled inverters are isolated from the bit lines BL and BLB. The data in the storage nodes remains unaltered. This mode is generally termed as standby mode and the power measured is static power or leakage power. If the stored bit is '0' (i.e., Q is discharged), the transistors M1, M5, M6 and M2, M7, M8 works as standard cross coupled inverters making the node QB charged to V_{DD}. In this case the stacked M7 and M8 are cut off. If the stored data is '1', QB is discharged to '0' and transistors M5 and M6 are cut-off. Since they are stacked transistors, the leakage current as well as the hold power will be highly reduced independent of the data value stored in this proposed structure.

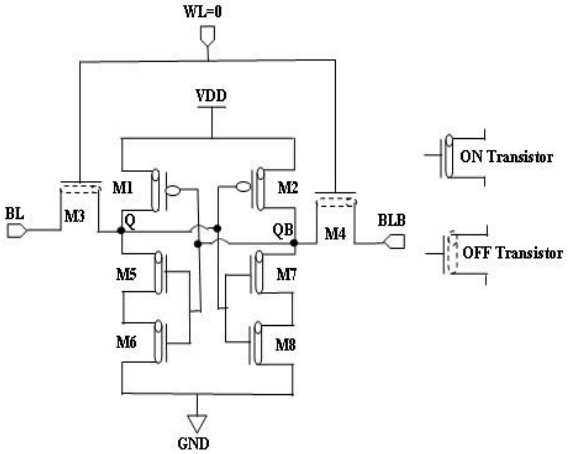

Fig. 6 P8TS SRAM in hold mode

2.2 Read State

Proposed SRAM read mode schematic is provided in Fig.7, wherein the bit lines BL and BLB are pre-charged

to the value of the supply voltage. The word line WL is asserted high so that the storage nodes get connected with the bit lines. In case of Q=1, the transistors M7 and M8 are '*on*', making the BLB line discharge through the path M4, M7 and M8. But the level of bit line BL remains same due to the '*off*' transistors M5 and M6. In case of Q=0, bit line BL is discharged through the '*on*' transistors M5 and M6. Sensing scheme can be utilized to detect the difference in the level of bit lines BL and BLB, which in turn implies the data value in the storage nodes.

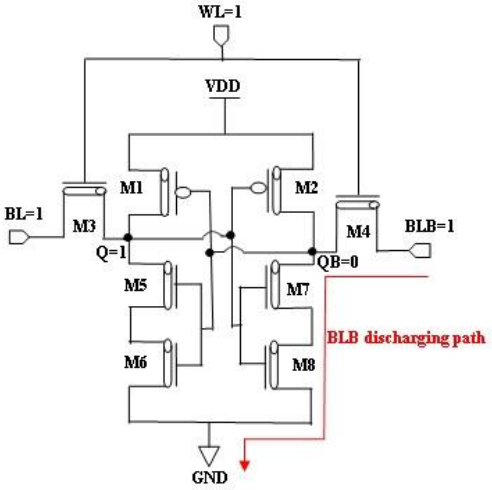

Fig. 7 P8TS SRAM in read mode

2.3 Write State

Write operation is initiated by raising the WL level to '1'. For successful write operation, the pull-down network on the side to be written '0' must be stronger than the pull up network that was holding the data'1'**.** Fig.8 presents the proposed memory structure during the write operation of data '1' and in this case two n-type CNFET make up the pull-down network and one P-type CNFET is on the pull up path. Let us assume that the cell is in hold state '0' that is Q is discharged and QB is charged. In order to write '1', BL is driven to high level and BLB is made low level, and the access transistors are tuned on. The node Q starts charging up thereby turning on the transistors M7 and M8, which in turn provides the discharge path for QB to decrease it to the level '0'.

3 Simulation results and analysis

The simulations are performed for the proposed structure and the conventional structures namely C8TRB and C7TRB SRAM, and the results are analyzed and compared in the following sections. Stanford university 32nm CNFET model [18] and HSPICE are utilized to perform the simulations and to estimate the power and delay in hold, read and write modes. Tabulation of the details of CNFET parameters and values used for simulation is provided in Table 1.

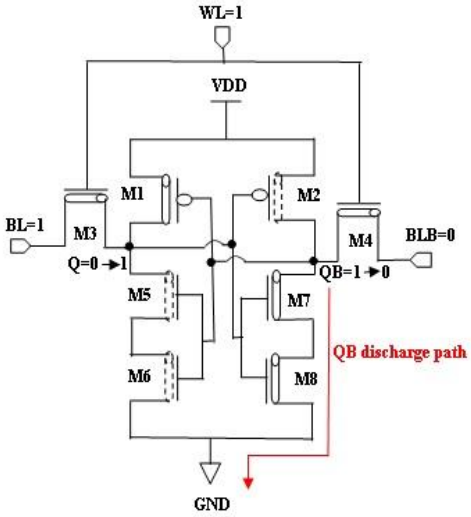

Fig. 8 P8TS SRAM in write mode

Read power is calculated by averaging the power consumed during a read '0' and read '1', similarly write power is the average of the power consumed during writing the data '0' and '1'. Write delay is considered as the time taken from asserting the word line to the time the storage node attains ninety percentage of the supply voltage. Read delay is assumed as the delay between the applying the word line and the bit line discharging to (V_{DD}-50mV). Power delay product is an important criterion for the analysis of VLSI circuits. It indicates the energy consumption of the conventional and proposed circuits.

The proposed memory structure is designed based on stacking technique. Stacking technique provides low power, but the limitation of stack effect is increased area and delay. In order to overcome the limitation of stacking technique, the sizing of the stacked transistor pair (M5, M6 and M7, M8) is optimized as per the Eq. (6)

$$W = (N-1)S + D_{CNT} \tag{6}$$

where *W*-transistor width, *N*-number of CNT tubes, *S*-pitch and D_{CNT}-CNT diameter. If the *W/L* ratio of unstacked transistor is considered as one, then optimization of the stacked transistor pair is done by halving W/L ratio.

Table. 1 CNFET Parameter and its values for simulation

S.No	Parameter	Value
1	Channel length (Lch)	32 nm
2	Intrinsic CNT channel mean free path (Lgeff)	100 nm
3	CNT source side extension region length (Lss)	32 nm
4	CNT drain side extension region length (Ldd)	32 nm
5	Dielectric constant of top gate dielectric material (Kgate)	16
6	Channel to substrate coupling capacitance (Csub)	40pF/m

Performance of the proposed technique with regard to power, speed and energy is tested for the variations in number of tubes, diameter, pitch and temperature. Fig.9, Fig.10 and Table 2 shows the effect of number of CNT tubes on SRAM power, delay and PDP. HPC8TRB, HPC7TRB, HPP8TS stands for hold power of the conventional 8T read buffer SRAM, conventional 7T read buffer SRAM and proposed 8T stacked SRAM respectively. Similar notations are used for read power, write power, read delay and write delay. Simulation results confirm Eq. (6) that if the CNT tubes in CNFET are increased, power consumption is elevating due to the change in transistor width. Here the tubes are changed from 3 to 15 and the proposed P8TS SRAM has 56% power savings compared to C8TRB SRAM, and a maximum of about 36% hold power, 50% read power and 99% write power savings is observed as that of C7TRB SRAM. The circuit speed of P8TS SRAM is improved by 27% and 97% whereas the PDP is decreased by 65% and 98% than C8TRB and C7TRB SRAM respectively. C7TRB SRAM has only seven transistors and its power, delay and PDP must be lower than the proposed structure. But simulation results prove that the proposed structure performs well than the C7TRB SRAM in spite of an additional transistor.

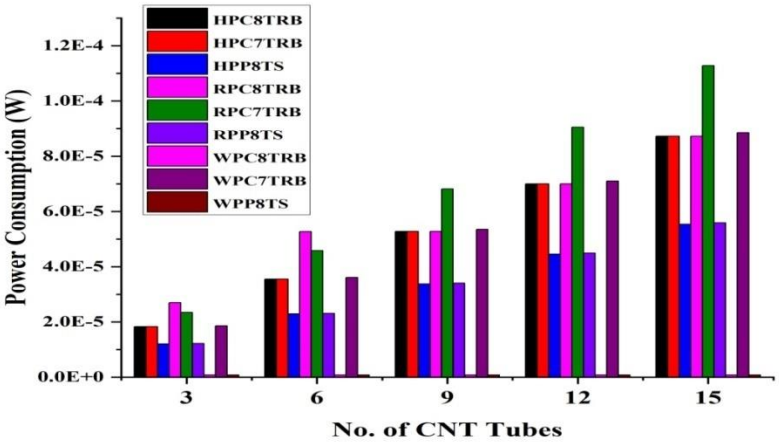

Fig. 9 Power consumption w.r.t change in tubes number

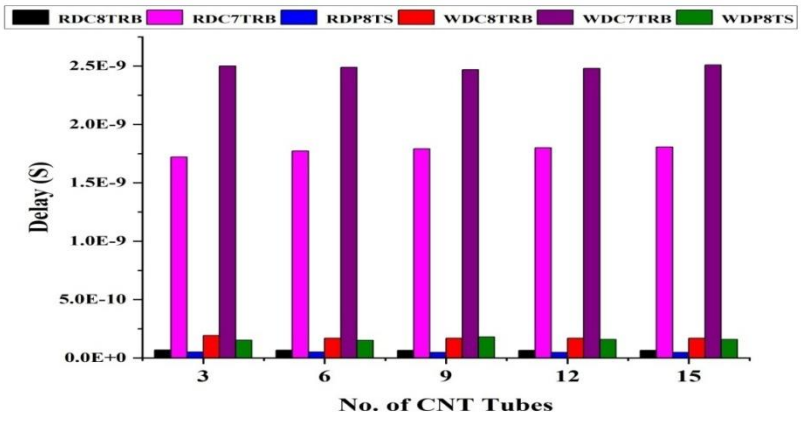

Fig. 10 Delay w.r.t change in tubes number

Table 2 PDP consumption w.r.t change in tubes number

SRAM	No. of CNT Tubes				
	3	**6**	**9**	**12**	**15**
Hold PDP (J)					
C8TRB	1.2427E-15	2.3542E-15	3.4656E-15	4.5768E-15	5.6880E-15
C7TRB	3.1460E-14	6.2991E-14	9.4519E-14	1.2605E-13	1.5758E-13
P8TS	**6.2299E-16**	**1.1810E-15**	**1.5961E-15**	**2.1065E-15**	**2.6169E-15**
Read PDP(J)					
C8TRB	1.8320E-15	3.4954E-15	3.4656E-15	4.5768E-15	5.6880E-15
C7TRB	4.0312E-14	8.1171E-14	1.2204E-13	1.6291E-13	2.0378E-13
P8TS	**6.2893E-16**	**1.1919E-15**	**1.6107E-15**	**2.1257E-15**	**2.6407E-15**
WritePDP(J)					
C8TRB	5.5084E-17	5.3719E-17	5.3253E-17	5.3022E-17	5.2888E-17
C7TRB	3.1935E-14	6.3936E-14	9.5933E-14	1.2793E-13	1.5993E-13
P8TS	**4.1816E-17**	**4.1812E-17**	**3.8382E-17**	**3.8356E-17**	**3.8344E-17**

Diameter and threshold voltage of CNFET are inversely proportional to each other as per Eq. (7). Increasing the diameter reduces the transistor threshold voltage, resulting in high power consumption and delay reduction. It is understood from Fig.11, Fig.12 and Table 3, that the P8TS SRAM power, delay and energy are lower than the conventional techniques even under diameter changes. Comparing the simulation results, P8TS SRAM minimizes 55% power, 76% delay and 92% PDP than C8TRB SRAM, and 97% power, 98% delay and 99% energy than C7TRB SRAM.

$$V_{th} = \frac{0.43}{D_{CNT}(nm)} \quad (7)$$

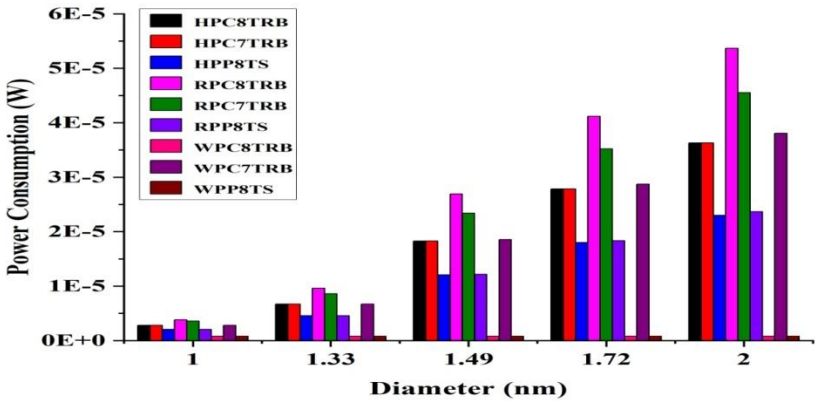

Fig. 11 Power consumption w.r.t change in tubes diameter

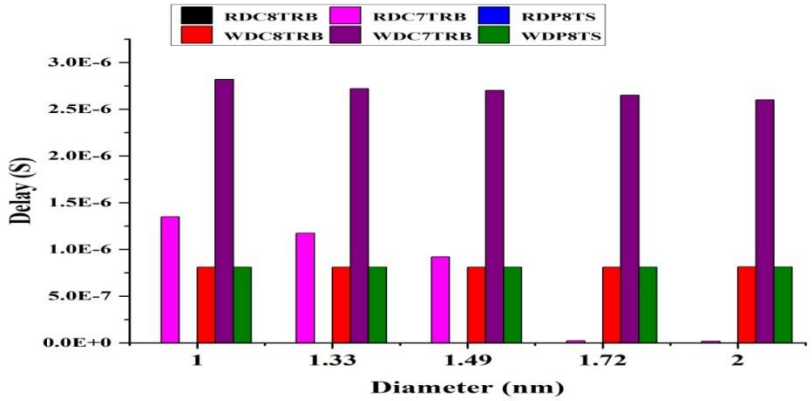

Fig. 12 Delay w.r.t change in tubes diameter

Table 3 PDP consumption w.r.t change in tubes diameter

SRAM	Diameter (nm)				
	1	**1.33**	**1.49**	**1.72**	**2**
Hold PDP (J)					
C8TRB	3.8326E-16	5.2427E-16	1.2427E-15	1.2587E-15	3.1803E-15
C7TRB	9.4408E-14	1.2553E-13	3.1460E-14	6.3638E-15	3.1719E-15
P8TS	**6.7316E-17**	**2.6805E-17**	**6.2299E-16**	**1.3609E-15**	**2.2116E-15**
Read PDP(J)					
C8TRB	5.1952E-16	7.5389E-16	1.8320E-15	1.8618E-15	4.7022E-15
C7TRB	1.1983E-13	1.6125E-13	4.0312E-14	8.0530E-15	3.9790E-15
P8TS	**6.7352E-17**	**2.6852E-17**	**6.2893E-16**	**1.3877E-15**	**2.2768E-15**
Write PDP(J)					
C8TRB	1.1013E-16	6.3374E-17	5.5084E-17	3.6663E-17	7.1221E-17
C7TRB	9.4451E-14	1.2579E-13	3.1935E-14	6.5684E-15	3.3264E-15
P8TS	**2.6379E-17**	**4.7533E-18**	**4.1816E-17**	**6.1260E-17**	**7.8124E-17**

Impact of pitch on power, delay and power delay product is provided in Fig.13, Fig.14 and Table 4. Even though the pitch of CNFET is directly proportional to power and inversely proportional to delay, its effect is minimal compared to the change in the number of tubes and diameter. Still, the proposed memory structure performance is better by 56% power, 25% delay and 65% PDP than C8TRB and 74% power, 97% delay and 99% energy than C7TRB SRAM.

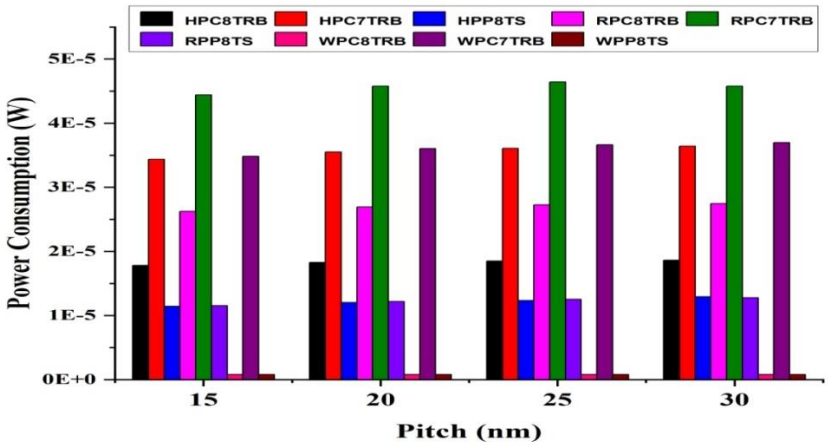

Fig. 13 Power consumption w.r.t change in pitch

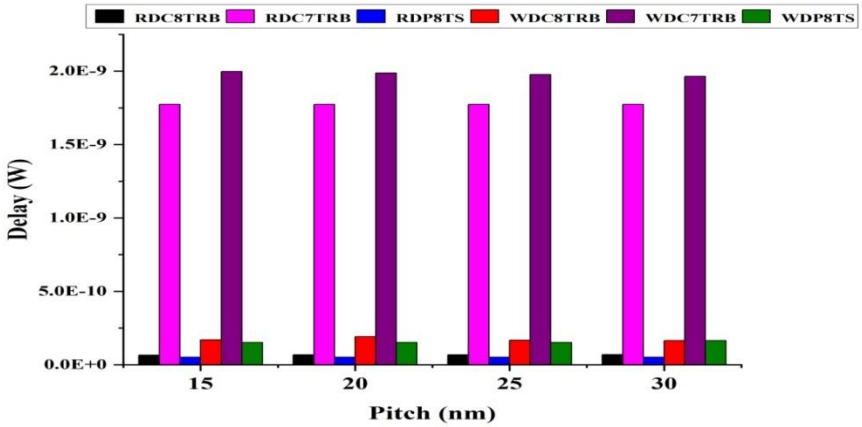

Fig. 14 Delay w.r.t change in pitch

Table 4 PDP consumption w.r.t change in pitch

SRAM	Pitch (nm)			
	15	20	25	30
Hold PDP (J)				
C8TRB	1.1782E-15	1.2427E-15	1.2743E-15	1.2920E-15
C7TRB	6.0943E-14	6.2991E-14	6.4005E-14	6.4575E-14
P8TS	**5.8836E-16**	**6.2041E-16**	**6.3818E-16**	**6.6989E-16**
Read PDP(J)				
C8TRB	1.7363E-15	1.8320E-15	1.8790E-15	1.9054E-15
C7TRB	7.8759E-14	8.1171E-14	8.2360E-14	8.1185E-14
P8TS	**5.9325E-16**	**6.2893E-16**	**6.4842E-16**	**6.6264E-16**
Write PDP(J)				
C8TRB	5.3566E-17	5.5084E-17	5.5797E-17	5.6186E-17
C7TRB	6.1785E-14	6.3936E-14	6.5004E-14	6.5604E-14
P8TS	**4.1648E-17**	**4.1816E-17**	**4.1908E-17**	**4.1963E-17**

Temperature is varied from 27°C to 100°C and the performances of the SRAM structures are analyzed. Fig.15, Fig.16 and Table 5 illustrates the effect of temperatures changes on power, delay and PDP respectively. Proposed P8TS SRAM has a reduction in 34% hold power, 54% write power, 24% delay and 65% energy compared to C8TRB SRAM, and decrease of about 96% read and write power, 97% delay and 98% energy is attained by P8TS SRAM than C7TRB SRAM. The prime interest of this paper is the analysis of power, delay and PDP of the proposed P8TS SRAM, but the RSNM (Read static noise margin) and WSNM (write static noise margin) are also evaluated and compared with the existing SRAMs. SNM represents static noise margin used to predict the performance of a circuit with regard to stability. Fig.17, Fig.18 and Fig.19 portrays the hold SNM, write SNM and read SNM butterfly curves, and it is obvious that the SNM of the proposed SRAM has comparable SNM apart from low power, delay and energy. The SNM values of the conventional and proposed structure are given in Table 6.

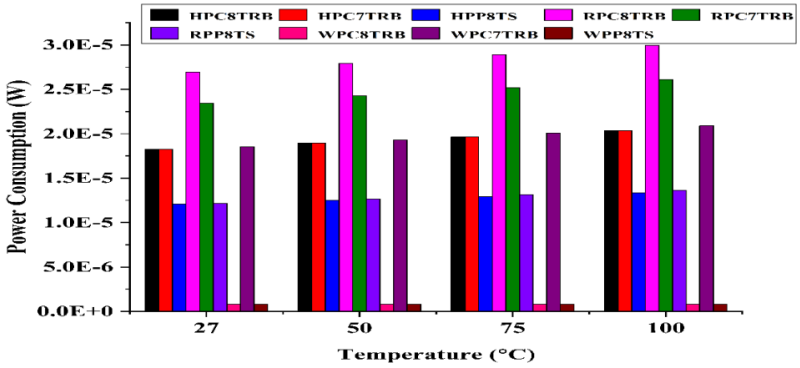

Fig. 15 Power consumption w.r.t change in temperature

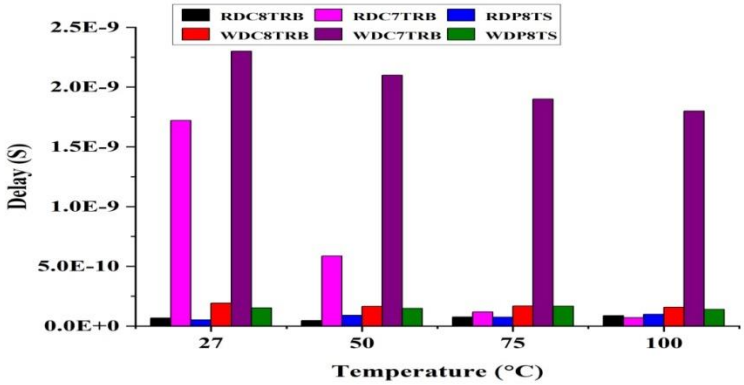

Fig. 16 Delay w.r.t change in temperature

Table 5 PDP consumption w.r.t change in temperature

SRAM	Temperature (°C)			
	27	**50**	**75**	**100**
Hold PDP (J)				
C8TRB	1.2427E-15	8.7139E-16	1.5040E-15	1.7827E-15
C7TRB	3.1460E-14	1.1108E-14	2.3257E-15	1.4390E-15
P8TS	**6.2299E-16**	**1.1297E-15**	**9.6638E-16**	**1.3106E-15**
Read PDP(J)				
C8TRB	1.8320E-15	1.2837E-15	2.2133E-15	2.6200E-15
C7TRB	4.0312E-14	1.4236E-14	2.9810E-15	1.8445E-15
P8TS	**6.2893E-16**	**1.1435E-15**	**9.8139E-16**	**1.3357E-15**
Write PDP(J)				
C8TRB	5.5084E-17	3.7288E-17	6.2078E-17	7.1159E-17
C7TRB	3.1935E-14	1.1314E-14	2.3780E-15	1.4771E-15
P8TS	**4.1816E-17**	**7.3314E-17**	**6.0589E-17**	**7.9566E-17**

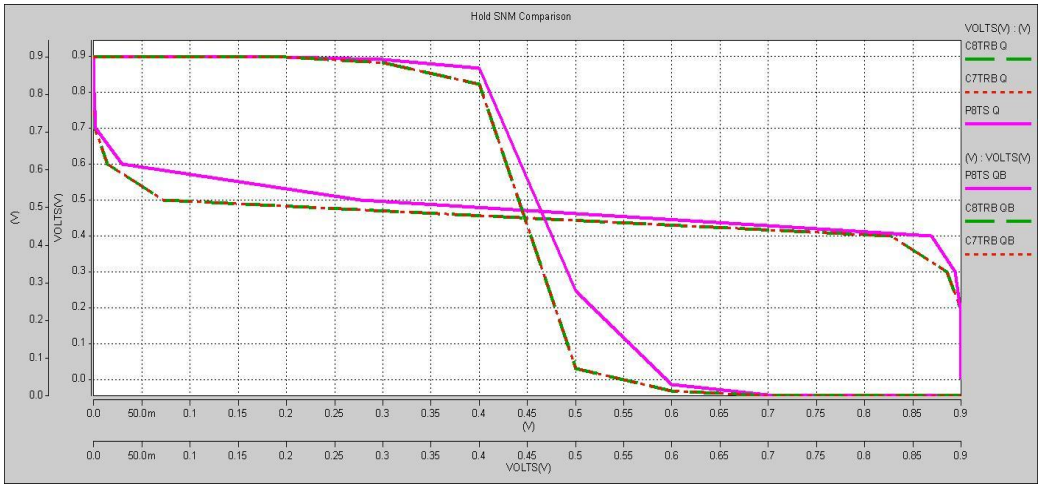

Fig. 17 HSNM Comparison

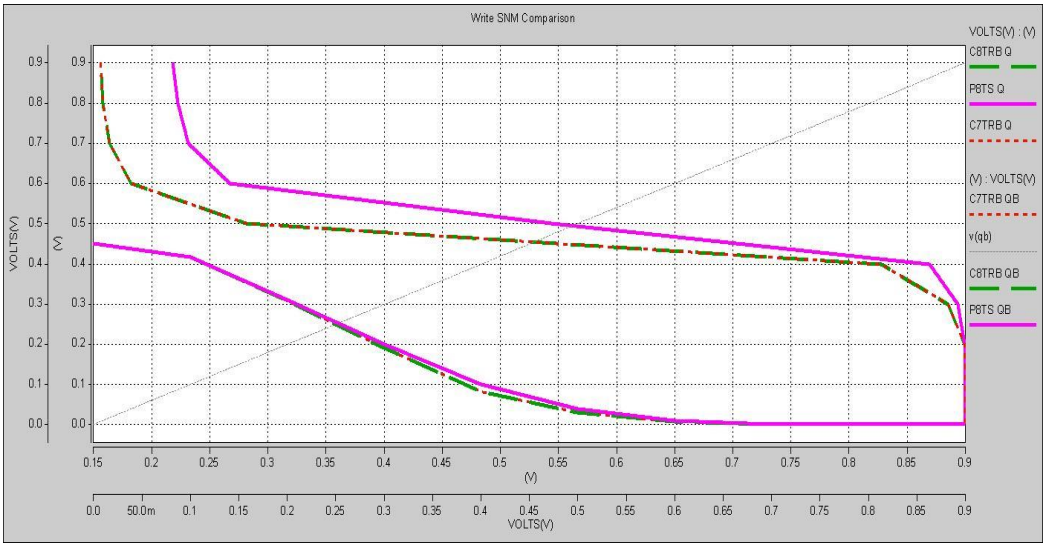

Fig. 18 WSNM Comparison

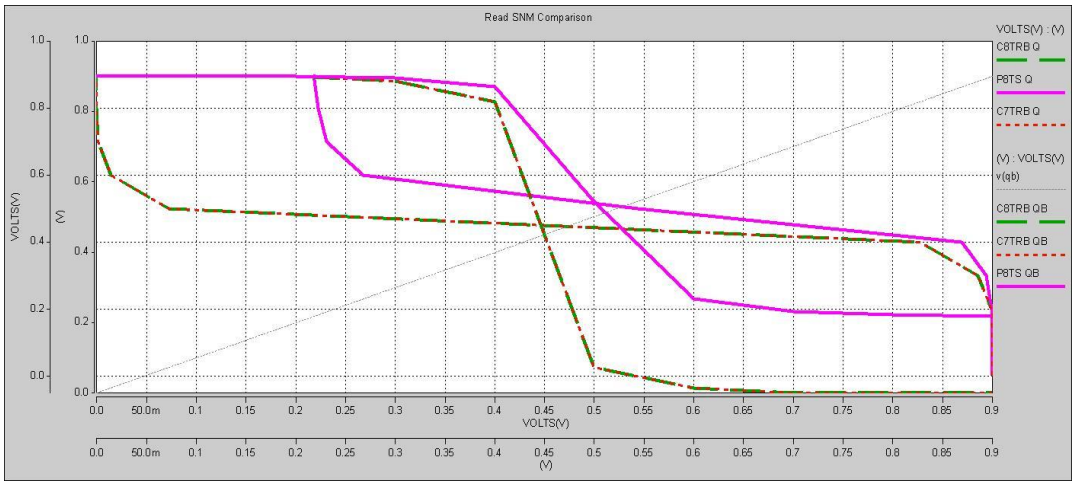

Fig. 19 RSNM Comparison

Table 6 SNM Comparison

SRAM	Hold SNM (V)	Read SNM(V)	Write SNM(V)
C8TRB	0.33519	0.323	0.357759
C7TRB	0.33619	0.324	0.359759
P8TS	0.32751	0.2782	0.346434

4 Conclusion

The power, delay and energy of the proposed 8T SRAM cell and conventional C8TRB and C7TRB SRAMs are compared and analyzed. To validate the performance of the proposed structure under various process variations, the number of CNT tubes, CNT diameter, pitch and temperature are changed, and simulations are carried out. It is observed that the proposed stacked 8T SRAM cell ensures high circuit speed, low power and energy even under process variations and confirms that it is a suitable structure for 5G networks by satisfying the major objectives like high speed, low power and low energy consumption.

Conflict of Interest

The authors declare no conflict of interest.

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