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Design and Performance Evaluation of a Novel Time Measurement Calibration Device for Electric Power Systems

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Abstract: In order to solve the difficulty of digital signal calibration of electric power equipment, such as low precision, inability to test the full range, and complicated configuration, and further promote the development of power system, a proposed time measurement calibration device is designed, and its performance is verified in this paper. This paper points out the main drawbacks of the existing calibration system, carries on the design innovation of the key technologies based on FPGA (Field Programmable Gate Array), puts forward the optimization method of the software and hardware, and verifies the accuracy of the input and output signal by experiments. The accuracy of input and output SV, GOOSE, and contact signal of the proposed calibration device in this paper can be better than 10μs, which is a meaningful improvement in accuracy and efficiency for time measurement calibration.

Keywords: Electric power equipment, time measurement, calibration, Field Programmable Gate Array

1 Introduction

WITH the development of smart grid and IEC 61850, the power system has entered the digital age, the application of digital equipment and tester has increased, and the accuracy requirements are becoming higher than before. Time measurement is an important function of electric power equipment, especially for the relay protection tester, which is responsible for accurately testing the response time or action time of relay protection or other electric power equipment. It mainly includes the digital signals such as SV (Sampled Value) and GOOSE (Generic Object Oriented Substation Event), and contact signals. In order to ensure the accuracy of time measurement, it is necessary to calibrate the equipment regularly according to the related standards. For instance, standard requirements for IEC 60255-151-2009, DL/T 1501-2016, DL/T 1944-2018 and T/CEC 247-2019 show that the time measurement accuracy of relay protection tester is ought to be better than 100μs [1-3].

However, at present, due to the lack of professional calibration device, manufacturers and organizations need to use a variety of equipment including recorder and assist relay protection device to build the temporary calibration system, which usually rely on the recorder and often introduce errors [4].

Moreover, there is also a gap in how to verify the error of calibration system experimentally. Some laboratories use contrast experiments to indirectly verify the error of the calibration device, which is not accurate enough.Based on the above challenges, this paper introduces the design of a new type of time measurement

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calibration device, and verifies its accuracy through experiments.

2 Analysis of Current Method

2.1 Time Measurement Requirement

There are six different types of time measurement, as shown in the Table 1 [4-5]. They are six combinations of three different kinds of signals (SV, GOOSE and hard contact signals).

Since there are no relevant technical standards and design standards for time measurement accuracy calibration in the power industry, this paper refers to the requirements of relay protection tester for time measurement accuracy test.

Table 1 Six types of time measurement

No.	Types	Range	Accuracy
1	From sending SV to receiving GOOSE	1ms ~ 99999ms	± 100μs (1ms<t≤100ms); ±0.1% (100ms<t≤99999ms)
2	From sending SV to receiving input contact signal		
3	From sending GOOSE to receiving GOOSE		
4	From sending GOOSE to receiving input contact signal		
5	From sending output contact signal to receiving GOOSE		
6	From sending output contact signal to receiving input contact signal		

According to the standard requirements in DL/T 1501-2016 "Technical specifications of digital test equipment for relay protection", DL/T 1944-2018 "Technical specifications of handheld optical digital signal test equipment in smart substation" and T/CEC 247—2019 "Technical specifications of digital-analog integrated test equipment for relay protection", the time measurement accuracy of relay protection tester is ought to be better than 100μs when the time measurement range is between 1ms and 100ms (1ms< t ⩽100ms); time measurement accuracy is ought to be better than ±0.1% when the time measurement range is between 1ms and 100ms (100ms< t ⩽99999ms) [4-6]. Therefore, if the accuracy of the proposed calibration device can be better than 10 μs, it will fully meet the calibration requirements.

2.2 Current Calibration Method

At present, it lacks effective methods to do the time measurement calibration in power industry. The existing calibration method is shown in Figure 1: Digital relay protection tester respectively input SV, GOOSE or hard open signal to relay protection device or other electric power equipment, relay protection device will process through its own functional logic after receiving the above signal, and then output the corresponding SV, GOOSE or contact signal, and then connect back to the digital relay protection tester. The digital relay protection tester calculates the time difference △T1 between the output signal and the access signal as a measurement value of the corresponding action time of the relay protection device. The recorder and analyzer device has the ability to access and time mark multiple SV, GOOSE, and contact signals. During the test, the recorder and analyzer device, as a third-party monitoring device, connects the output of the relay protection tester, the output of the relay protection device, and marks the time. The time difference △T2 between the output signal of the relay protection tester and the output signal of the relay protection device can be calculated by using the time marker of the recorder and analyzer device, as the actual value of the corresponding action time. Calculate the measurement error of △T=△T1-△T2, and △T as the error of the time measurement of relay protection tester [7].

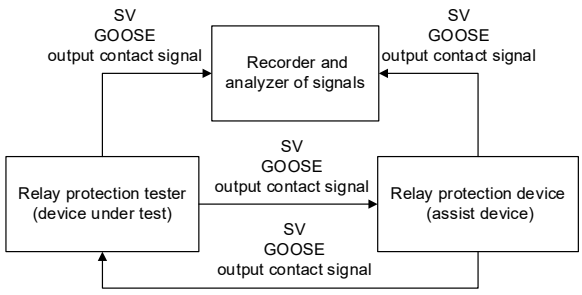


Fig 1. Existing calibration method diagram [2]

2.3 Drawbacks of Current Calibration Method

The existing calibration methods mainly have the following drawbacks:

i. Low precision: It is completely dependent on external recorder and relay protection device. The recorder and relay protection device used in calibration are limited by their own performance, and the accuracy of the action time is relatively low (millisecond level), and the fluctuation is large, and the measurement error of calibration will be affected by the fluctuation, which

increases the difficulty of analysis and reduces the accuracy of calibration [8].

ii. Cannot be verified at full range: The action time of relay protection device is fixed and cannot be adjusted, and the full range (1ms-100s) cannot be simulated [9].

iii. Complex configuration: It needs to use a variety of equipment to build the temporary calibration system, and the recorder and relay protection device are complicated to build and configure [10-11].

3 Key Technologies of the Proposed System

This paper designed a calibration device for precise calibration for time measurement of electric power equipment. Since FPGA device is superior to microcontroller in speed and anti-interference, and the FPGA could be used to implement frequency modulation and phase locking with IRIG-B signal source, and is able to implement high-precision adjustment of internal clock, and could provide accurate time beat for each module, the FPGA is used to achieve accurate input and output control [12-16].

3.1 Accurate Time Calibration of Input Data

High precision internal clock management is the cornerstone of time measurement accuracy detection and calibration [17-18]. The frequency modulation and phase locking with the IRIG-B signal source are realized through the FPGA device, and the internal clock is adjusted with high precision to provide accurate time beats for each module. When the proposed device is connected to an external clock source, the clock logic calculates the difference between internal and external clocks in real time, and uses the error approximation algorithm to accurately adjust the local clock to ensure the synchronization of internal time rhythms.

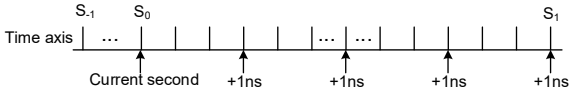


Fig 2. Accurate time calibration of input data

Example: If the time difference between the previous second and the local system time is 100ns, the system adjusts the time by 100ns in the next second. Firstly, the adjustment position is calculated. For example, the 100MHz clock is adjusted once every 1milion clocks, that is, 1ns is increased.

(1) Contact signal accurate receiving

For contact signal, FPGA device performs high frequency sampling and real-time comparison of switching input voltage. When the on-in voltage exceeds the threshold value of the change, time calibration is carried out immediately. After processing the logic such as de-jitter, the initial change moment is backtracked, and the change moment time marker is taken as the exact change time marker.

(2) Optical port message receiving

For the optical port message receiving, the FPGA device monitors the PHY (Physical Layer) device of the network port, calibrates the arrival time of the leading byte of the network message, and calibrates the hardware delay of the optical port according to the parameters set by the system, so as to accurately obtain the time mark of the message arrival.

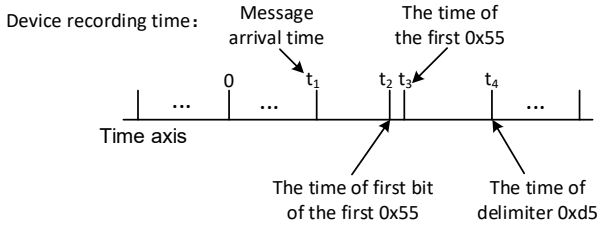


Fig 3. Proposed time calibration method for receiving messages

The calibration method of receiving message time is shown in Figure 7. As shown in the figure, t1 is the time when the message arrives at the device, and t3 is the time of the first 0x55 of the message. And t4 is the moment at which the packet frame begins delimiter 0xd5. The time is traced back to the moment when t2 is the first bit of the packet leader 0x55, and the hardware delay is corrected. Get the real time t1 when the packet arrives at the device, that is, the timestamp of the frame packet.

3.2 Accurate time calibration of output data

The proposed calibration device can achieve accurate time output control for SV, GOOSE and contact signals, mainly including the following two aspects.

(1) Contact signal accurate output

Using quick output node, using special front hardware to control, reduce the uncertainty of front hardware delay. The bottom drive delay and hardware delay in the slicing time interval are compensated by the FPGA device, and the upper logic delay is compensated by the front-end system software.

(2) Optical port message output

FPGA optimizes and implements network MAC layer logic to directly control network PHY devices, and can accurately evaluate the time interval between network data preparation and actual transmission. When the FPGA obtains the data packet from the bus queue, it extracts the time label, and compensates the logical delay and hardware time to obtain the time that really needs to be written into the network PHY, then monitors the current time in real time, and accurately writes the network

message at the specified time to complete the accurate time transmission.

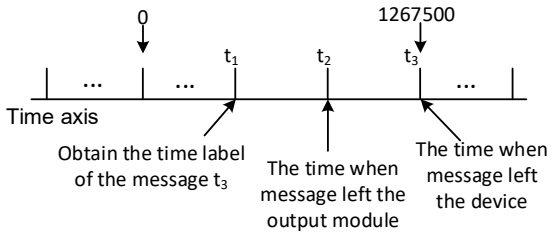


Fig 4. Proposed control logic of message sending time

Example: A frame is required to be sent at 1267500ns in the current second. The data processing module obtains the message and time label to be sent at t1. If the hardware delay takes 80ns, to ensure that the message leaves the device at t3=1267500ns, it is necessary to control the message to leave the message output module at t2=1267420ns.

3.3 High precision action time setting

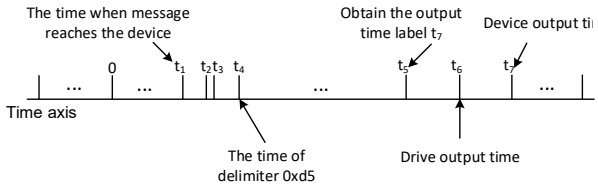


Fig 5. Proposed method of high precision action time setting

Based on accurate input and output, the action time setting can be realized. The detection and calibration device records the arrival time t1 of the incoming message according to the accurate time calibration method of the incoming message. At the same time, the output module obtains the output time label t7 at t5, and drives the output at t6 according to the logic time of the output module and the output hardware delay, so as to ensure that the contact output is effective at t7, and t7- t1 is the operation time △ T.

4 Implementation of the Proposed System

The calibration device proposed in this paper realizes the closed-loop calibration of time measurement process through special hardware design and software design.

4.1 Proposed System Framework

The calibration system framework is shown in the figure 6. The relay protection tester outputs SV, GOOSE or contact signals to the proposed calibration device, and the proposed calibration device outputs feedback signals to the relay protection tester after a set time delay (i.e. operation time).

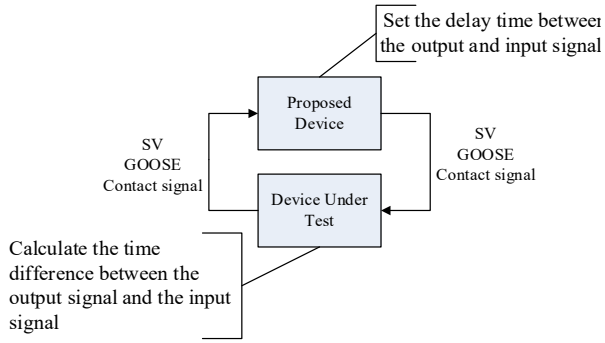


Fig 6. Framework of proposed time measurement calibration system

4.2 Proposed Hardware Design

The proposed device's hardware structure includes the following modules: The configuration module, The message receiving module, The data processing module, The message sending module. As shown in figure 7.

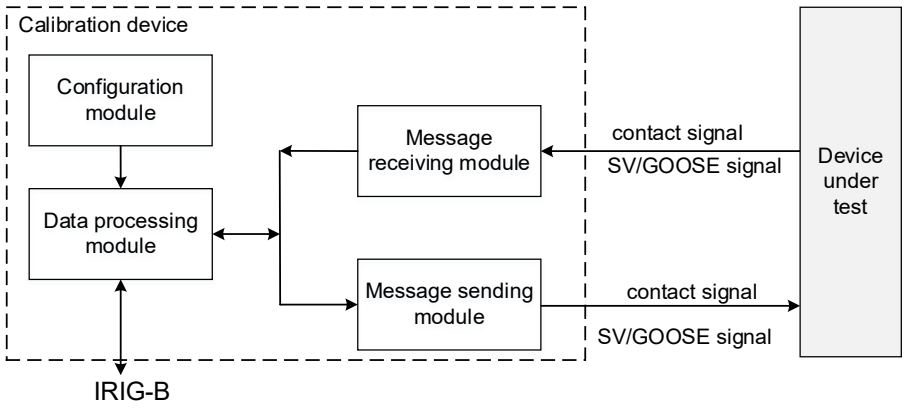


Fig 7. Hardware design diagram of the proposed calibration device

(1) The configuration module

The configuration module completes the parameter information configuration of SV and GOOSE signals, contact on/off configuration information, etc., and completes the delay time configuration between the output signal and the input signal as required.

(2) The message receiving module

The message receiving module collects the SV and GOOSE signals output by the device under test, marks them accurately and sends them to the data processing module. The fast access module collects the open and open signals of the hard contact output of the device under test and sends them to the data processing module after accurately marking the time mark.

(3) The data processing module

The data processing module analyzes the incoming and outgoing signals of SV, GOOSE or contact signals, analyzes the input time of the signal, and calculates the sending time of the incoming and outgoing signals of SV, GOOSE or contact signals according to the configured delay time. Then the signal sending time is sent to the message sending module.

(4) The message sending module

The message sending module sends SV, GOOSE or contact signals according to the configured network port, delay time, sending time and other configuration. Configuration and input/output display diagram of proposed system is shown in figure 8.

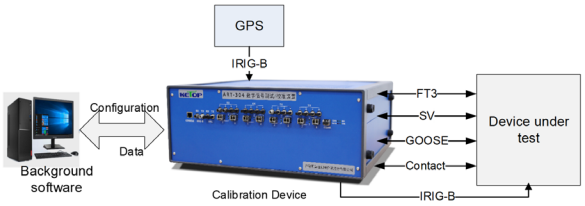


Fig 8. Configuration and input/output display diagram of proposed system

4.3 Proposed Software Design

The proposed calibration device's software uses modular and hierarchical design. It mainly includes the driver layer, the interaction layer, and the logic layer.

The following figure 9 is one of the software test cases of the proposed calibration device combined with the schematic diagram, and here taking the GOOSE signal as an example.

Step 1: The digital relay protection tester outputs GOOSE signal Gos1.

Step 2: The proposed calibration device receives the GOOSE signal Gos1 sent by the digital relay protection tester and marks the time mark T1′ accurately.

Step 3: The proposed calibration device output GOOSE signal Gos2 at time T1′+ 100 μs according to the set delay time △T1=100 μs.

Step 4: The digital relay protection tester receives the GOOSE signal Gos2, and calculates the time difference △T2 between the output of the digital relay protection test and the receipt of the signal.

Step 5: Calculate △T=△T2-△T1 to determine whether the error exceeds the requirements of the relevant technical standards of the digital relay protection tester.

Step 6: Change △T1 in Step 3 to the required time of 1ms, 100ms, 1s, 50s, and 100s, and repeat Step 1 to Step 5.

GOOSE signal Gos1 and GOOSE signal Gos2 described in the embodiments are only examples.

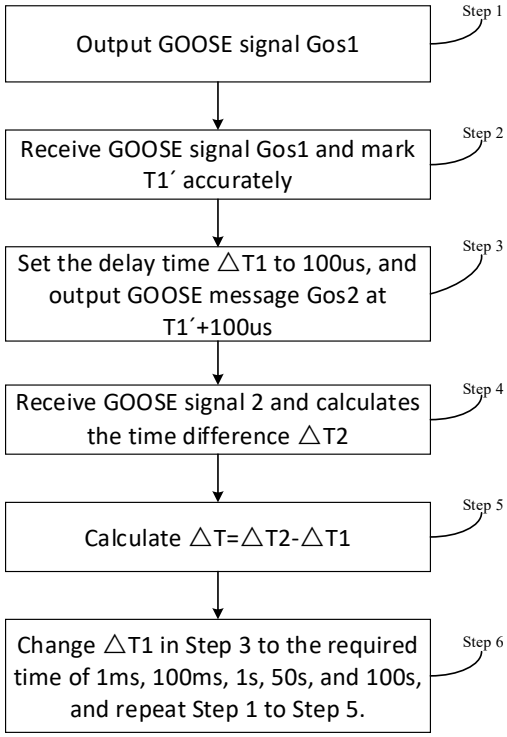


Fig 9. One example of the test cases of the proposed calibration device

5 Performance Analysis

In this paper, a special accuracy verification system is set up to test the input and output accuracy of the proposed calibration device. The proposed verification system is shown in Figure 10. When the proposed calibration device and the relay protection tester

perform closed-loop testing, the contact signal is connected to the oscilloscope in parallel for monitoring, and the digital signal (SV or GOOSE) is connected to the recorder and analyzer in parallel for monitoring, so as to achieve the accuracy verification of the input and output signals.

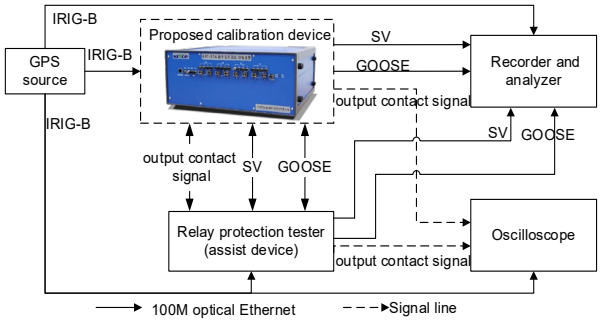


Fig 10. Diagram of the proposed calibration device's accuracy verification structure

Since the time measurement accuracy of the relay tester is required to be 100 μs, the accuracy of the proposed calibration device can be fully competent for calibration if it can reach 10 μs [2].

5.1 Accuracy Verification of Input Data

The relay protection tester periodically sends SV, GOOSE or contact signal, the proposed calibration device records the signal arrival time as T1, the recorder or oscilloscope records the signal arrival time as T2, and T1-T2 is the error of the input signal. Each kind of signal was tested 500 times, and the statistics and analysis results were shown in Table 2. The mean value, maximum value, minimum value, and standard deviation were calculated. According to the test results, even the maximum error can still meet the calibration requirements (better than 10μs).

Table 2 Data analysis for accuracy of input signals

Data type	Recommended values	Error			
		Minimum	Mean	Maximum	*Standard deviation*
SV	10μs	30ns	58.5ns	79ns	10.34ns
GOOSE		38ns	56.7ns	74ns	8.4ns
Contact signals		1.685μs	2.798μs	3.728μs	0.551μs

5.2 Accuracy Verification of output Data

The proposed calibration device is set to send SV, GOOSE or contact signal at T1, and the recorder or oscilloscope records the arrival time of the signal at T2, and T1 - T2 is the error of the output signal. Each kind of signal was tested 500 times, and the statistics and analysis results are shown in Table 3. The mean value, maximum value, minimum value, and standard deviation were calculated. According to the test results, even the maximum error can still meet the calibration requirements (better than 10 μs).

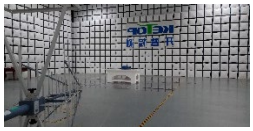
Table 3 Data analysis for accuracy of output signals

Data type	Recommended values	Error			
		Minimum	Mean	Maximum	Standard deviation
SV	10μs	34ns	56.8ns	75ns	10.2ns
GOOSE		33ns	56.4ns	79ns	9.5ns
Contact signals		0.968μs	1.329μs	1.962μs	0.259μs

5.3 Anti-interference verification

Considering that in addition to the laboratory, the detection and calibration device is also applied to the industrial production environment, its anti-interference capability is verified by referring to the electromagnetic compatibility requirements of standards IEC 60255-22-3: 2007, IEC 60255-22-4: 2008, IEC 60255-22-1:2007, IEC 60255-25: 2000, and DL/T 1501-2016, and the results are shown in the following Table 4 [19-21].

Table 4 Result of EMC test

No.	Test Item	Test Requirement	Picture	Verdict
1	Pulse group interference	Severity Rating: Level 3		Pass
2	Electrostatic discharge interference	Severity Rating: Level 3		Pass
3	Radiation electromagnetic field interference	Severity Rating: Level 3		Pass
4	Fast transient interference	Severity Rating: B		Pass
5	Conducted emission limit	The conducted emission value within 150KHz ~ 30MHz does not exceed the standard requirements		Pass
6	Radiation emission limit	The radiation emission value within 30MHz ~ 1GHz does not exceed the standard requirements		Pass

6 Conclusion

The proposed calibration device in this paper solves the problem of the lack of effective calibration methods for the time measurement accuracy of the electric power equipment. The accuracy of input and output SV, GOOSE and contact signal of the proposed calibration device in this paper is better than 10μs. The device proposed in this paper has the full range(1ms-100s) calibration, and closed-loop testing can be achieved without complex configuration. Compare that with other calibration system, the proposed calibration device is a meaningful improvement in accuracy and efficiency for time measurement calibration. The proposed calibration device is suitable for calibration institutions, testing institutions and power equipment manufacturing enterprises to solve industry problems. What's more, the method of design and performance analysis of this proposed calibration device can also be used for reference by other fields of electrical equipment.

In order to achieve the target of engineering application, the accuracy of the proposed device is verified by performance test experiments, and the maturity and reliability are verified by anti-interference experiments, which proves that the proposed device and technology have practical value and engineering prospect.Conflict of Interest

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Y. Huang: Designing the study, writing-original draft; H. N. Afrouzi: Revising the first draft, conceptualization, reviewing; C-L. Wooi: Editing, reviewing; H. T. Su: Supervision, editing; I. Hijazin: Validation, reviewing.

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Biographies

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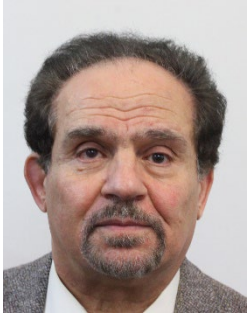

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