Single DV-DXCCII Based Voltage Controlled First Order All-Pass Filter with Inverting and Non-Inverting Responses

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Abstract: In this paper, a new voltage controlled first order all-pass filter is presented. The proposed circuit employs a single Differential Voltage Dual-X second generation Current Conveyor (DV-DXCCII), a NMOS (n-type Metal Oxide Semiconductor) transistor operated in the triode region as an active resistor and a grounded capacitor. The proposed all-pass filter provides both inverting and non inverting voltage-mode outputs simultaneously from the same configuration without any matching constraint. Non-ideal analysis along with sensitivity analysis is investigated. The proposed circuit has low active and passive sensitivities. The Monte Carlo analysis is also done for showing good sensitivity performances of the proposed circuit. In addition, to utilize the feature of cascadability, an application of higher order filter is also given. Moreover, the use of grounded capacitor makes the proposed circuit particularly attractive for Integrated Circuit (IC) implementation point of view. The theoretical results are validated through PSPICE simulations with TSMC 0.18 μm Complementary Metal Oxide Semiconductor (CMOS) process parameters.

Keywords: All-Pass Filter, Dual-X Current Conveyor, First Order, Voltage-Mode.

1 Introduction

All-pass filters are widely used to shift the phase of the signal while keeping its amplitude constant over the desired frequency range. Thus all-pass filters can correct the undesired change in phase during analog filtering operations. The literature survey shows that several first-order all-pass filter (APF) circuits using different types of active building blocks such as second generation current-controlled current conveyor (CCCII) [1], differential voltage current conveyor (DVCC) [2- 4, 7, 8, 10], inverting voltage buffer (IVB) [9], operational transconductance amplifier (OTA) [5, 6, 8, 11], second generation current conveyor (CCII) [13, 17, 25], third generation current conveyor (CCIII) [14], differential difference current conveyor (DDCC) [15, 29], dual-X second generation current conveyor (DXCCII) [19, 23], current conveyors (CC) [16], current differencing buffered amplifier (CDBA) [17], fully differential second generation current conveyor (FDCCII) [20, 30], universal voltage conveyor (UVC) [6, 22], voltage differencing inverting buffered amplifier (VDIBA) [24], Extra-X current controlled conveyor (EX-CCCII) [26], differential difference dual-X second generation current conveyor (DD-DXCCII) [27], current controlled conveyor transconductance amplifier (CCCTA) [28] have been reported. A study of some recently published first-order voltage mode all-pass filters based on single active element is presented in this section [11-30]. The filter circuits presented in [11-20, 22, 23, 25, 29, 30] require more than one passive components to realize first-order APF and few of them also require matching condition [11-14, 17, 19, 22, 25, 29]. However, the circuits presented in [11, 15, 16, 18, 20, 23, 30] are based on one active element and two passive components. The reported circuits do not require any matching condition. In order to add the tunability in the existing circuits, a resistorless realization can be implemented by replacing the resistor with a MOSFET based voltage controlled resistor. Recently, the resistorless voltage mode first-order all-pass filter based on single active element was presented in [21, 24, 26-28]. However, the circuit presented in [24, 27, 28] employs floating capacitor. It is well known fact that a floating capacitor can be realized as double poly layer. However the grounded IC capacitors have less parasitics compared to floating counterparts, which is significant from the performance point of view [33]. Table 1 presents a comparison of some of the reported first order voltage-mode all-pass filter based on single active element.

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Table 1 Comparison study of the existing single active element based voltage-mode all pass filter circuits with the proposed circuit.

Ref. No.	Type of Used Active Element*	Passive Components Count	Resistorless Realization Shown	No Passive/ Active Matching Constraints	Feature of Tunability	Feature of Grounded Capacitors used	Inverting and Non-Inverting All-Pass Responses, Simultaneously
11	OTA	2	Yes	No	Yes	No	No
12	CCII	5	No	No	No	Not in all	No
13	CCII	3	No	No	No	No	No
14	CCIII	4	No	No	No	No	No
15	DDCC	2	No	Yes	No	No	No
16	CC	2	No	Yes	No	Yes	No
17	CCII	3	No	No	No	Yes	No
18	CDBA/CCCDBA	2	No	Yes	No	No	No
19	DXCCII	4	No	No	No	Yes	No
20	FDCCII	2	No	Yes	No	Yes	No
21	VD-DIBA	1	Yes	Yes	Yes	Yes	No
22	UVC	3	No	No	No	No	Yes
23	DXCCII	2/3	No	Yes	No	Not in all	No
24	VDIBA	1	Yes	Yes	Yes	No	Yes
25	CCII	3	No	No	No	Yes	No
26	EX-CCCII	1	Yes	No	Yes	Yes	No
27	DD-DXCCII	1	Yes	Yes	Yes	No	No
28	CCCTA	1	Yes	No	Yes	No	No
29	DDCC	4	No	No	No	Yes	No
30	FDCCII	2	No	Yes	Yes	Yes	No
Proposed	**DV-DXCCII**	**1**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**

* *Abbreviations:* OTA: Operational Transconductance Amplifier, CCII: Second Generation Current Conveyor, CCIII: Third Generation Current Conveyor, DDCC: Differential Difference Current Conveyor, CC: Current Conveyor, CDBA: Current Differencing Buffered Amplifier, CCCDBA: Current Controlled Current Differencing Buffered Amplifier, DXCCII: Dual-X Second Generation Current Conveyor, FDCCII: Fully Differential Second Generation Current Conveyor, VD-DIBA: Voltage Differencing Differential Input Buffered Amplifier, UVC: Universal Voltage Conveyor, VDIBA: Voltage Differencing Inverting Buffered Amplifier, EX-CCCII: Extra-X Current Controlled Conveyer, DD-DXCCII: Differential Difference Dual-X Second Generation Current Conveyor, CCCTA: Current Controlled Conveyor Transconductance Amplifier, DV-DXCCII: Differential Voltage Dual-X Second Generation Current Conveyor.

This paper presents a new voltage controlled first order all-pass filter (VC-APF) based on differential voltage dual-X second generation current conveyor (DV-DXCCII). The proposed circuit employs a single DV-DXCCII, a NMOS transistor operated in the triode region and a grounded capacitor. The proposed circuit provides both inverting and non-inverting all-pass responses simultaneously at two different terminals without any matching constraint. The feature of low output impedance at the one output terminal is also explored by realizing an nth order VC-APF. It can be noticed from the comparison Table 1 that none of the reported circuits realized a tunable first order voltage mode all-pass filter with both inverting and non-inverting all-pass responses simultaneously from the same circuit by employing a single active element, an active resistor and a grounded capacitor.

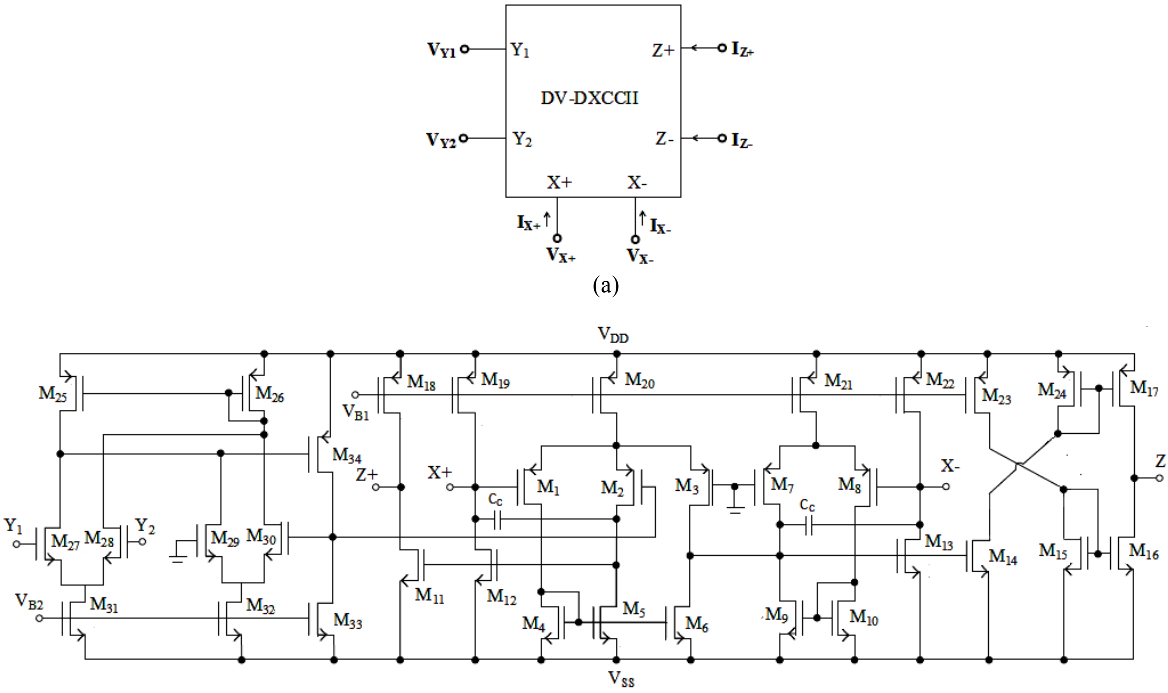
2 Proposed Circuit

DV-DXCCII is a six terminal analogue building block which is characterized by the following port relations

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_{X+} \\ V_{X-} \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ -1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_{X+} \\ I_{X-} \end{bmatrix} \tag{1}$$

DV-DXCCII combines the advantages of the DVCC [31] and DXCCII [32]. The symbol and the CMOS implementation of DV-DXCCII is shown in Fig. 1(a) and Fig. 1(b), respectively. The CMOS implementation of Fig. 1(b) comprises of DVCC (M_{25}–M_{34}) with unemployed Z-stages and DXCCII (M_1–M_{24}). In the CMOS implementation of DV-DXCCII, the X-terminal (gate of M_{30}) of DVCC drives the Y-terminal (gate of M_2) of the DXCCII.

The Z+ and Z- stages are realized from the drain of M_{11} and M_{16} transistors. The DV-DXCCII has two high impedance input terminals (Y_1 and Y_2), two low impedance terminals (X+ and X-) and two high impedance output terminals (Z+ and Z-).



(a)

(b)

Fig. 1 (a) Symbol of DV-DXCCII (b) CMOS implementation of DV-DXCCII.

The proposed voltage controlled first-order all-pass filter (VC-APF) is shown in Fig. 2. The proposed circuit consists of a single DV-DXCCII, an NMOS transistor biased in the triode region and a grounded capacitor. The proposed circuit is characterized by the following two transfer functions for inverting (V_{out1}) and non-inverting (V_{out2}) filter responses.

$$\frac{V_{out1}}{V_{in}} = -\left(\frac{sCR_{MOS}-1}{sCR_{MOS}+1}\right) \tag{2}$$

$$\frac{V_{out2}}{V_{in}} = \left(\frac{sCR_{MOS}-1}{sCR_{MOS}+1}\right) \tag{3}$$

where, R_{MOS} is the resistance of the NMOS transistor in Fig. 2 and is given by

$$R_{MOS} = \left[\mu C_{ox}\left(\frac{W}{L}\right)(V_G - V_T)\right]^{-1} \tag{4}$$

where, μ_n, C_{ox}, V_T, W and L are the surface mobility, oxide capacitance, threshold voltage, channel width and the channel length of NMOS.

The phase responses of the transfer functions (Eqs. (2) and (3)) are to be found as

$$\phi_1 = -2\tan^{-1}(\omega R_{MOS}C) \tag{5}$$

$$\phi_2 = 180^o - 2\tan^{-1}(\omega R_{MOS}C) \tag{6}$$

From Eq. (2) and Eq. (3), the pole frequency can be expressed as

$$\omega_o = 1/R_{MOS}C \tag{7}$$

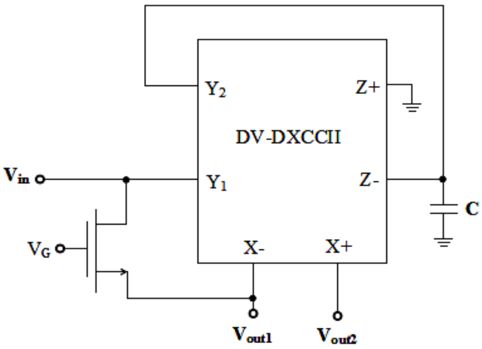


Fig. 2 Proposed voltage controlled first-order all-pass filter.

From Eq. (7), it is evident that the pole frequency can be easily controlled by adjusting the gate voltage of the NMOS transistor.

3 Non-Ideal Analysis

Taking the non-idealities associated with the DV-DXCCII into account, the relationship of the terminal voltages and currents of the DV-DXCCII can be expressed as:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_{X+} \\ V_{X-} \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & 0 & 0 \\ -\beta_3 & \beta_4 & 0 & 0 \\ 0 & 0 & \alpha_1 & 0 \\ 0 & 0 & 0 & -\alpha_2 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_{X+} \\ I_{X-} \end{bmatrix} \tag{8}$$

where, β_1 and β_2 are the voltage transfer gains from the Y_1 terminal to the X+ terminal and Y_2 terminal to the X+ terminal, respectively, β_3 and β_4 are the voltage transfer gains from the Y_1 terminal to the X- terminal and Y_2 terminal to the X- terminal, respectively. α_1 is the current transfer gain from the X+ terminal to the Z+ terminal and α_2 is the current transfer gain from the X- terminal to the Z- terminal.

Using Eq. (8) ideal transfer functions of the proposed first order VC-APF will be modified as the following transfer functions.

$$\frac{V_{out1}}{V_{in}} = -\left(\frac{\beta_3 sCR_{MOS} - \alpha_2\beta_4}{sCR_{MOS} + \alpha_2\beta_4}\right) \tag{9}$$

$$\frac{V_{out2}}{V_{in}} = \left(\frac{\beta_1 sCR_{MOS} + \alpha_2\beta_1\beta_4 - \alpha_2\beta_2(1+\beta_3)}{sCR_{MOS} + \alpha_2\beta_4}\right) \tag{10}$$

The phase responses of the transfer functions (Eq. (9) and Eq. (10)) are to be found as

$$\phi_1 = -\tan^{-1}\left(\frac{\omega\beta_3 R_{MOS}C}{\alpha_2\beta_4}\right) - \tan^{-1}\left(\frac{\omega R_{MOS}C}{\alpha_2\beta_4}\right) \tag{11}$$

$$\phi_2 = 180^o + \tan^{-1}\left(\frac{\omega\beta_1 R_{MOS}C}{\alpha_2\beta_1\beta_4 - \alpha_2\beta_2(1+\beta_3)}\right) - \tan^{-1}\left(\frac{\omega R_{MOS}C}{\alpha_2\beta_4}\right) \tag{12}$$

From Eq. (9) and Eq. (10), the pole frequency can be expressed as

$$\omega_o = \frac{\alpha_2\beta_4}{R_{MOS}C} \tag{13}$$

The active and passive sensitivities with respect to ω_o are given as below

$$S_{\alpha_2}^{\omega_o} = S_{\beta_4}^{\omega_o} = -S_{R_{MOS}}^{\omega_o} = -S_{C}^{\omega_o} = \frac{1}{2} \tag{14}$$

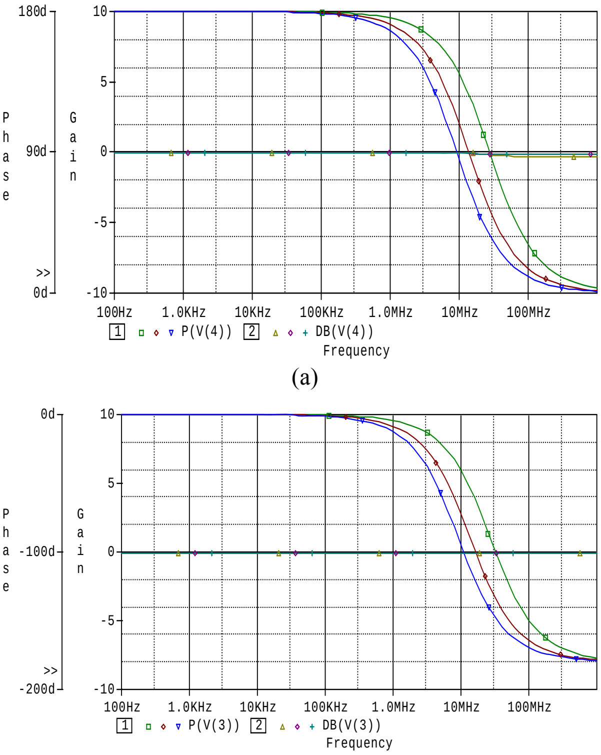
The sensitivities of active and passive components with respect to pole frequency (ω_o) are within unity in magnitude. Thus, the new circuit of first order all-pass filter enjoys attractive active and passive sensitivity performance.

4 Simulation Results

The first order VC-APF of Fig. 2 is simulated using the CMOS implementation of DV-DXCCII with 0.18 µm device parameters, the supply voltages used were ± 0.9 V and V_{B1} = -0.37 V and V_{B2} = -0.6 V. The aspect ratios of the MOS transistors used in the simulation are given in Table 2. The transistor aspect ratio for the MOS based active resistor (R_{MOS}) is selected as 14.4µm/0.18µm. The proposed circuit was designed with C = 5 pF and gate control voltages (V_G) as 0.62 V, 0.65 V and 0.71 V. The simulated gain and phase responses are shown in Fig. 3 which depicts the variation in pole frequency at different gate voltages.

Table 2 Aspect ratios of MOS transistors used for simulation.

Transistors	**W(µm)/L(µm)**
M_1-M_2, M_4-M_5, M_{17}-M_{26}	1.44/0.18
M_3, M_6-M_{10}	2.88/0.18
M_{11}-M_{16}	11.51/0.18
M_{27}-M_{30}	0.29/0.18
M_{31}-M_{32}	5.22/0.18
M_{33}	16.19/0.18
M_{34}	3.6/0.18

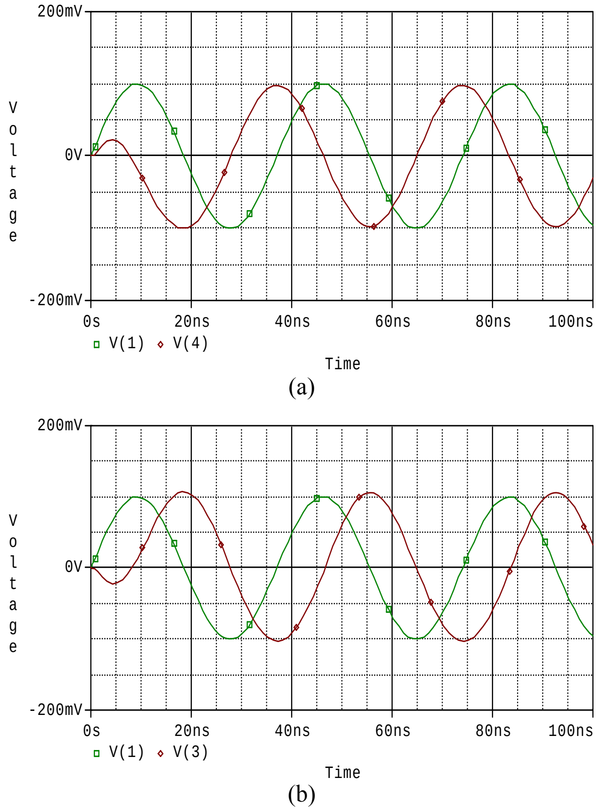


(a)

(b)

Fig. 3 Simulated gain and phase responses of VC-APF (a) Inverting (V_{out1}) (b) Non-Inverting (V_{out2}).

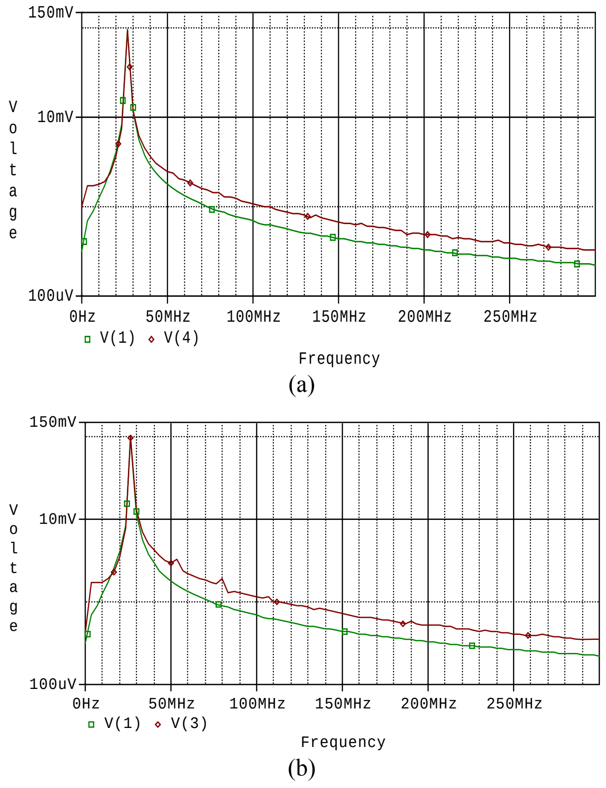
It has been observed from Fig. 3 that the pole frequencies at V_{out1} are found to be 10.34 MHz, 15.02 MHz and 27.13 MHz and at V_{out2} are found to be 10.23 MHz, 14.82 MHz and 27 MHz. Next to show the voltage swing capability and phase errors, the transient analysis is executed on the proposed circuit at 27 MHz. The simulated input and output waveforms are shown in Fig. 4. It is shown from the results that output waveforms are +90^0 and -90^0 phase shifted with the input waveform as expected. Fig. 5 shows the Fourier spectrum of the output waveforms at 27 MHz. In addition, the X–Y pattern (Lissajous pattern) for the two outputs with +90^0 and -90^0 phase shifts is also illustrated in Fig. 6.



(a)

(b)

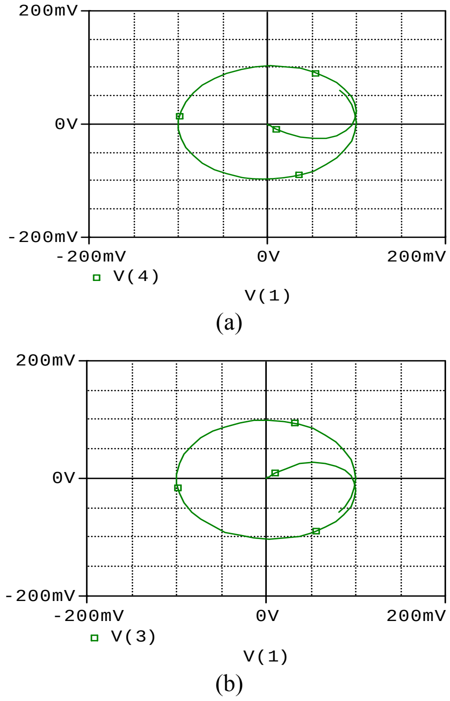
Fig. 4 Input/output waveforms for first-order VC-APF at 27 MHz (a) Inverting (V_{out1}) (b) Non-Inverting (V_{out2}).



(a)

(b)

Fig. 5 Fourier spectrum of input-output waveforms at 27 MHz (a) Inverting (V_{out1}) (b) Non-Inverting (V_{out2}).

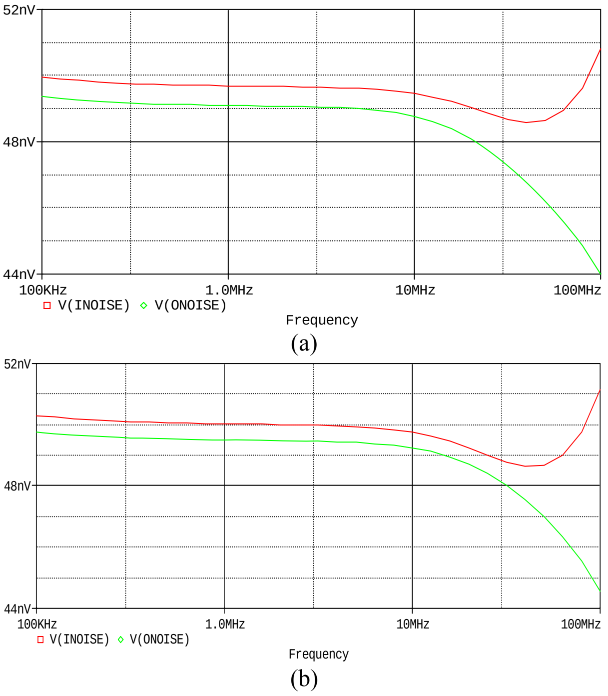


(a)

(b)

Fig. 6 X-Y pattern (a) showing +90^0 phase shift for V_{out1} and -90^0 phase shift for V_{out2} against input voltage at 27MHz.

The input and output noise spectral densities for both responses with respect to frequency are shown in Fig. 7. The equivalent input/output noises are found to be 48.78/47.56 nV/√Hz for V_{out1} and 48.97/48.61 nV/√Hz for V_{out2}, respectively.



(a)

(b)

Fig. 7 Input and output noise variations against frequency for (a) Inverting (V_{out1}) (b) Non-Inverting (V_{out2}).

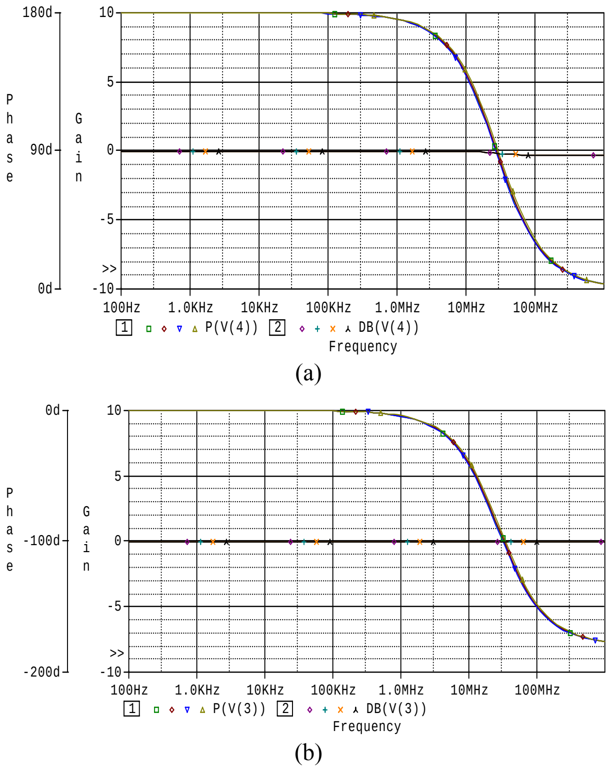


Fig. 8 Frequency responses at different operating temperatures (a) Inverting (V_{out1}) (b) Non-Inverting (V_{out2}).

Next, study on the proposed first-order VC-APF is carried out on its temperature performance, the simulated frequency responses at operating temperature range i.e. -40° C to 120° C are shown in Figs. 8(a) and 8(b) for V_{out1}, and V_{out2}. Figs. 8(a) and 8(b) shows that the phase shift is found to vary with frequency while the magnitudes remain almost invariable.

In addition, the Monte Carlo analysis of the proposed circuit of Fig. 2 is done for multiple runs while parameters (the threshold voltage, V_{T0} and the process transconductance parameter, K'n) are varied. The Monte Carlo simulation can be done for a Uniform or Gaussian probability distribution. V_{T0} and K'n are endorsed to follow a Gaussian deviation of 15% for nominal 10 runs, each varying independently. The gain and phase responses of proposed VC-APF with Monte Carlo analysis with the variations in V_{T0} are shown in Fig. 9. Also, Fig. 10 shows the variation in the gain and phase responses with the deviation in K'n. As depicted from the outcomes of Monte-Carlo analysis, the proposed VC-APF has good sensitivity performances.

5 nth Order Voltage Controlled All-Pass Filter

All-pass filters have a unit magnitude response over all the frequencies with the phase change. Therefore, they can be used to realize an nth order all-pass filter which can be used as an analog group delay equalizers for the video and communication applications [34]-[35].

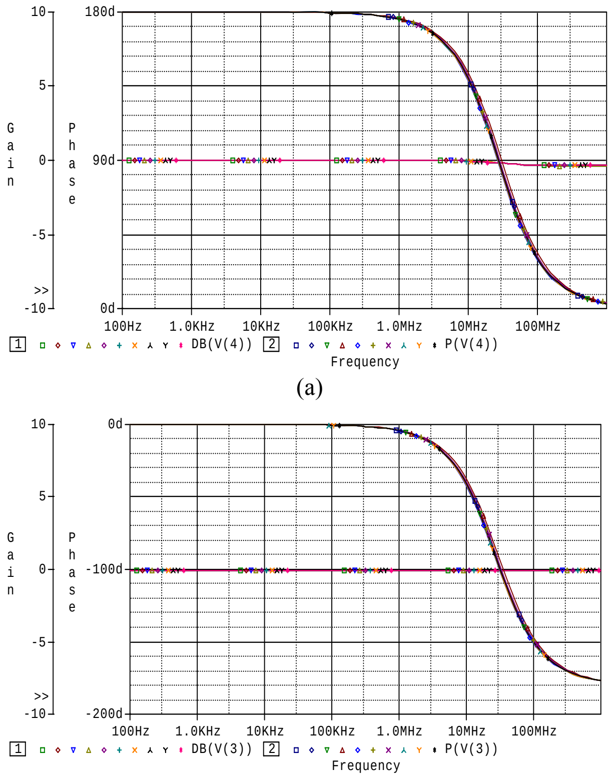


Fig. 9 Monte Carlo analysis with the variations in V_{T0} showing all-pass response (a) Inverting (V_{out1}) (b) Non-Inverting (V_{out2}).

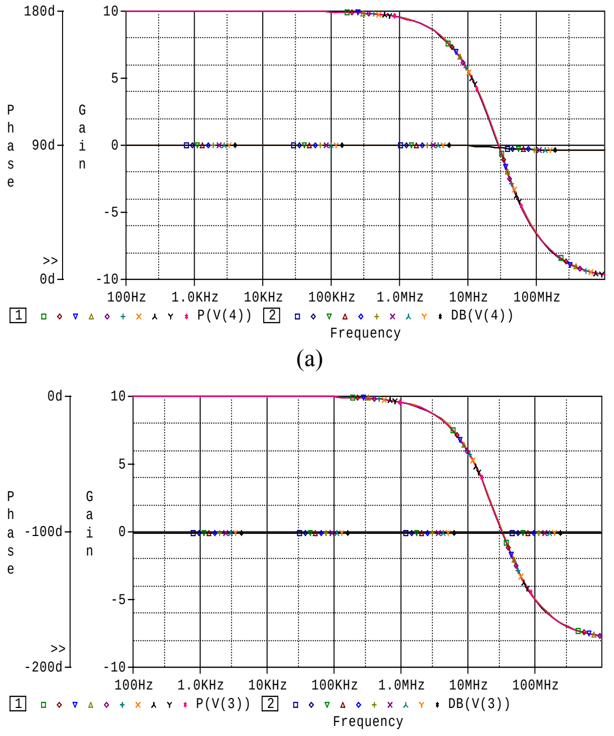


Fig. 10 Monte Carlo analysis with the variations in K'n showing all-pass response (a) Inverting (V_{out1}) (b) Non-Inverting (V_{out2}).

The nth order all-pass filter is realized by connecting the n-number of first-order all-pass filters in cascade [36]. By exploiting the feature of the first-order VC-APF i.e. the availability of one output V_{out2} at low output impedance terminal, an nth order filter is further realized as shown in Fig. 11. The proposed nth order VC-APF employs n-stages of DV-DXCCII, n-NMOS transistor biased in the triode region and n-grounded capacitors.

Analysis of the proposed circuit of Fig. 11 yields the following two transfer functions.

$$\frac{V_{out1(n)}}{V_{in}} = (-1)^n\left(\frac{sC_1R_{MOS1}-1}{sC_1R_{MOS1}+1}\right)\times\left(\frac{sC_2R_{MOS2}-1}{sC_2R_{MOS2}+1}\right)\times \cdots\cdots\times\left(\frac{sC_nR_{MOSn}-1}{sC_nR_{MOSn}+1}\right) \tag{15}$$

$$\frac{V_{out2(n)}}{V_{in}} = \left(\frac{sC_1R_{MOS1}-1}{sC_1R_{MOS1}+1}\right)\times\left(\frac{sC_2R_{MOS2}-1}{sC_2R_{MOS2}+1}\right)\times \cdots\cdots\times\left(\frac{sC_nR_{MOSn}-1}{sC_nR_{MOSn}+1}\right) \tag{16}$$

The angular resonance frequency ($\omega_{o(n)}$) can be expressed as

$$\omega_{o(n)} = \left(\frac{1}{(C_1C_2........C_n)\times(R_{MOS1}R_{MOS2}........R_{MOSn})}\right)^{\frac{1}{n}} \tag{17}$$

To illustrate the utility of the proposed nth order VC-APF, a third-order all-pass filter circuit is implemented with n = 3 (three DV-DXCCII, three NMOS transistors and three grounded capacitors). Putting n = 3 in Eq. (15) and Eq. (16), the two transfer functions are modified as

$$\frac{V_{out1(3)}}{V_{in}} = (-1)^3\left(\frac{sC_1R_{MOS1}-1}{sC_1R_{MOS1}+1}\right)\times\left(\frac{sC_2R_{MOS2}-1}{sC_2R_{MOS2}+1}\right)\times\left(\frac{sC_3R_{MOS3}-1}{sC_3R_{MOS3}+1}\right) \tag{18}$$

$$\frac{V_{out2(3)}}{V_{in}} = \left(\frac{sC_1R_{MOS1}-1}{sC_1R_{MOS1}+1}\right)\times\left(\frac{sC_2R_{MOS2}-1}{sC_2R_{MOS2}+1}\right)\times\left(\frac{sC_3R_{MOS3}-1}{sC_3R_{MOS3}+1}\right) \tag{19}$$

Equation (18) and (19) are the third-order inverting and non-inverting all-pass transfer functions. The angular resonance frequency $\omega_{o(3)}$ by putting n = 3 in eq. (17) is given by

$$\omega_{o(3)} = \left(\frac{1}{(C_1C_2C_3)\times(R_{MOS1}R_{MOS2}R_{MOS3})}\right)^{\frac{1}{3}} \tag{20}$$

The third-order all-pass circuit is designed by taking $C_1 = C_2 = C_3 = 5$ pF and gate control voltage $V_{G1} = V_{G2} = V_{G3} = 0.62$ V, 0.71 V and 0.8 V. The simulated gain and phase responses are shown in Fig. 12 which shows the variation in angular resonant frequency at different gate voltages. It can be seen that the pole frequency at $V_{out1(3)}$ are found to be 10.32 MHz, 14.97 MHz and 27.02 MHz and at $V_{out2(3)}$ are found to be 10.13 MHz, 14.62 MHz and 26.92 MHz.

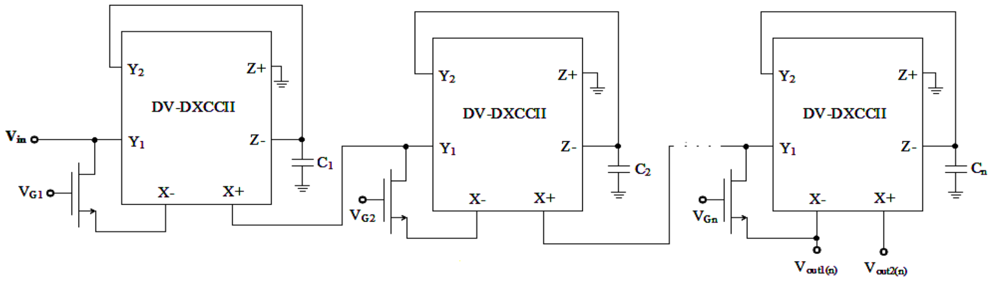
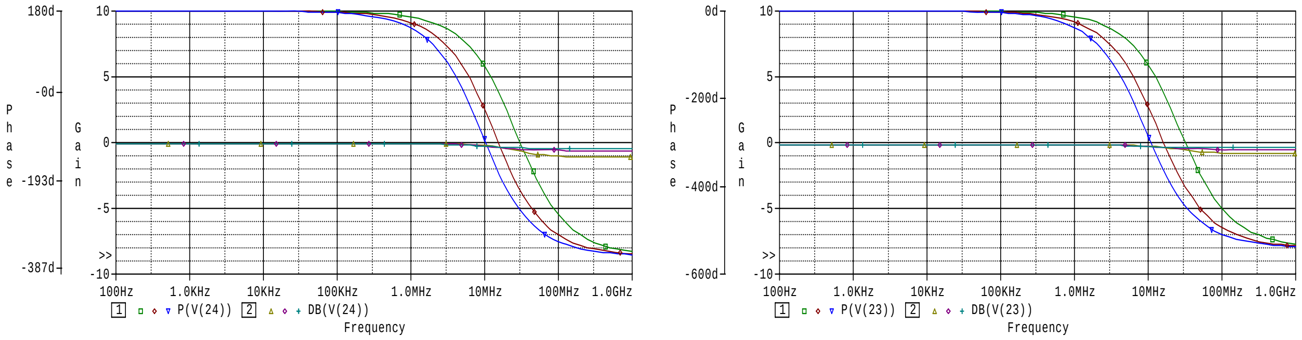


Fig. 11 nth-order voltage controlled all-pass filter.



(a) (b)

Fig. 12 Simulated gain and phase responses of third order VC-APF (a) Inverting ($V_{out1(3)}$) (b) Non-Inverting ($V_{out2(3)}$).

6 Conclusion

A new voltage controlled first order all-pass filter, employing single DV-DXCCII as active component, one NMOS transistor biased in triode region and one grounded capacitor as passive component is proposed. The given circuit enjoys the features of resistorless structure, use of grounded capacitor, use of single active element, minimum components requirement for first order all-pass filter, inverting and non-inverting all-pass responses simultaneously and controlling of filter pole frequency through external voltage. Non-ideal analysis is also discussed. As an application, an n^{th} order all-pass filter employing the proposed filter connected in cascade is also presented. The circuits are found to show good frequency performance, which makes them superior to existing works. Simulations results are given to confirm the presented theory.

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