A Novel Very High Performance CMOS Current Mirror with Extremely Low Input and Ultra High Output Resistance

H. Faraji Baghtash*, S. J. Azhari** and Kh. Monfaredi**

Abstract: In this paper a novel very high performance current mirror is presented. It favorably benefits from such excellent parameters as: Ultra high output resistance (36.9GΩ), extremely low input resistance (0.0058Ω), low output (~0.18V) and low input voltage (~0.18V) operation, very low power consumption (20μW), very low offset current (1pA), ultra wide current dynamic range (150dB), and ultra high accuracy (error = 0.003%). The circuit has a very simple compact architecture and uses a single 1V power supply. The qualitative performance of the circuit is validated with HSPICE simulations using HSPICE TSMC 0.18μm CMOS, BSIM3 and Level49 technology.

Keywords: Current Mirror, Extremely Low Input Resistance, Low Voltage, Low Power, Ultra High Accurate, Ultra High Output Resistance.

1 Introduction

Technology down scaling introduces great advantages into the performance of both digital and analog integrated circuits. It is well known that shrinking the transistor feature size increases intrinsic speed of device, and lowers power supply and power consumption.

Furthermore low power circuit design is increasingly in demand due to its extremely importance for portable applications. However technology down scaling besides the low power supply constrains also introduces such other demerits as: reduced dynamic range, reduced output impedance and reduced gain in circuits. Current mirror is one of the most important and widely used building blocks in VLSI designs. It is used to perform current amplification, level shifting, biasing and active loading. It can be found many researches dealt with problems of low voltage current mirrors' designs [1]-[8]. Also some low voltage design techniques such as using body driven, multi floating gate transistors, sub threshold and self cascode schemes are introduced in literature [9]. The common widely used low voltage current mirror is the well known low

voltage cascode current mirror (LVCCM) as is shown in Fig. 1. It has rather high input and output compliance, moderately low input and high output resistance, and high accuracy [10]. The modified version of the cited current mirror that provides lower input impedance and higher input compliance is shown in Fig. 1(b) (in which the input current is separated from bias current and applied to drain of mirror transistor M1).

However this modification degrades accuracy and current dynamic range. Furthermore this scheme introduces some offset current to the circuit. The offset current can be removed (i.e. as is removed in the current work) but the accuracy and dynamic range problems still exist. This is due to the fact that there is a difference between currents of cascode transistors M1C and M2C. These two versions of LVCCM are reviewed in [10], [11]. This problem can be moderated by using regulated cascode version of the circuit which employs an amplifier to compare drain source voltage of mirror
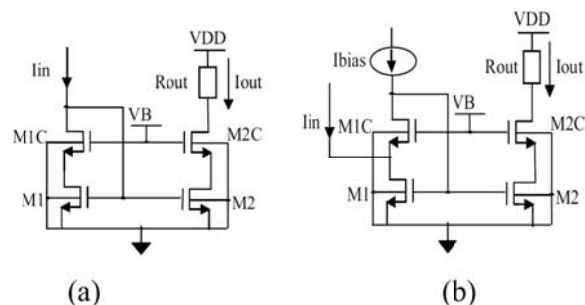

Fig. 1 (a) The well known low voltage cascode current mirror. (b) The improved version known as Flipped Voltage Follower (FVF) [10].

transistors making them to equal and results in improvement of current copying accuracy [12].

In [12] a current mirror is presented that achieves higher performance by utilizing regulated cascode scheme. It benefits from a scheme uses an amplifier on the output side to increase output impedance and accuracy. But its input impedance, which is another important parameter of the current mirror, still is not sufficiently low.

The conventional method to achieve low input impedance is using shunt negative feedback in input side. Favorably there are many topologies that use not only shunt feedback in input side, but also series one in output side [13]-[15] resulting both low input and high output resistances plus accuracy of the current mirrors. To be more precise, [13] uses two nested shunt feedback loops on the input side such that one of which is implemented by a flipped voltage follower (FVF) [16] and the other one consists of an amplifier A1 and transistor M1C. Both loops act simultaneously to reduce the input impedance. In [13] a single ended common source amplifier is used to implement A1 and A2. These amplifiers have gains $A1=A2=g_m r_o$. The limitation of this circuit is that, VGS of M1C and M2C must be less than threshold voltage of MA1 and MA2 to allow MA1 and MA2 transistors to operate in saturation mode. This might not be possible in some CMOS technologies. This problem is rather alleviated in [10] but some other specifications as input impedance and accuracy are not sufficiently improved. Fig. 2(c) shows a compact high gain implementation of the current mirror scheme of Fig. 2(a) in which NMOS cascode amplifiers are used for A1 and A2 [14]. These amplifiers use the lowest rail voltage as reference voltage V_{ref} which, in this case (Fig. 2(c)), is equal to the level shifted voltage at the positive input terminals of A1 and A2. The auxiliary amplifiers have, in this case, gains of A1, A2~ $(g_m r_o)^2$ that lead to extremely low input resistance and extremely high output resistance. A limitation of this implementation is that the minimum input and output voltages are relatively large compared to those of the conventional FVF mirror: $V_{in,min}=V_{GSA1}$, $V_{o,min}=V_{GSA2}$ $+V_{DSsatM2C}$. For this reason the circuit is not appropriate to be used in low supply environment required by modern CMOS technologies. It is also difficult to maintain M1C in saturation unless a level shifter is used in the FVF feedback loop [13]. Other implementations of amplifiers are introduced in [14], [15] which provide two extremely low input impedances for the related current mirror; 0.012 and 0.01 ohm, respectively. But [15] suffers from circuit complexity and higher power consumption. Also the circuit proposed in [14] uses floating gate transistors in its feedback loop which has its limits and needs a more expensive technology to be implemented [17], [18].

Hence in this work a very high performance current mirror is proposed which benefits from a simple compact power efficient circuit. Furthermore it does not use expensive technologies like floating gate technology. Mean while it provides most of outstanding merits one may expect from a current mirror with excellent performance ,those are; ultra low input impedance, ultra high output impedance, very high input and output compliances, ultra wide current dynamic range, extremely low current transfer error and current offset.

2 Principal of Operation

In Figure 3 the proposed cascode current mirror is shown. It is an all cascode scheme using special amplifiers A1 and A2 which are composed of transistors MA11 to MA14 and MA21 to MA24, respectively while Vb provides the bias voltage of their middle transistors. The top and bottom transistors of amplifiers configure inverter and the middle ones are arranged in cascode structure to increase the output resistances of the inverters for a significant gain. Using inverter as an amplifier eliminates the mentioned disadvantages of [13]. Also, on the contrary of Fig. 2(c), this scheme eliminates the input and output voltage limitations. Furthermore the implementation of this circuit is very simpler than other previously proposed circuits due to elimination of current source networks for central part (MA11-MA24), and does not need to use the expensive floating gate technology. Moreover, this scheme removes the offset problem by subtracting I_b from I_{out} via I_b current source placed at output branch. Besides, this current source (i.e. I_b) increases the ratio of current transfer to next following stage which is very important in signal processing. However when the circuit is used only for biasing purposes, this current mirror, is replaced by a subsystem/subcircuit/element which is aimed to be biased. The gain of the proposed amplifiers are A1, A2~ $(g_m r_o)^2$ as can be found in more detailed by
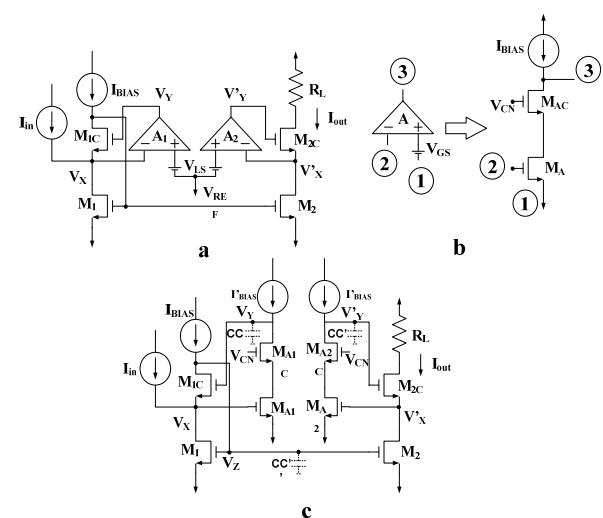

Fig. 2 Double nested regulated cascode current mirror (a) implementation of auxiliary amplifiers A1 and A2 (b) all cascode mirror (c) [13].

relations (1) and (2), using small signal analysis of the amplifiers.

$$A1 = \frac{(g_{mA11}+g_{mA14})}{\left(\dfrac{g_{dsA12}g_{dsA11}}{g_{mA12}}+\dfrac{g_{dsA13}g_{dsA14}}{g_{mA13}}\right)} \qquad (1)$$

$$A2 = \frac{(g_{mA21}+g_{mA24})}{\left(\dfrac{g_{dsA22}g_{dsA21}}{g_{mA22}}+\dfrac{g_{dsA23}g_{dsA24}}{g_{mA23}}\right)} \qquad (2)$$

Assuming similar transistors are used in each amplifier causes (1) and (2) to be simplified as (3) and (4), respectively:

$$A1 = \mu_{11-12} \cdot \mu_{13-14} \qquad (3)$$

$$A2 = \mu_{21-22} \cdot \mu_{23-24} = A1 \qquad (4)$$

Performing small signal analysis for proposed current mirror the input and output resistances can be obtained from (5) and (6) respectively.

$$R_{in} = \frac{g_{ds3}}{g_{m1}g_{m3}A1} \qquad (5)$$

$$R_{out} = \frac{g_{m4}A2}{g_{ds2}g_{ds4}} \qquad (6)$$

3   Simulation Results

HSPICE simulations of the proposed current mirror are carried on using TSMC 0.18μm CMOS, BSIM3 and Level49 technology with single 1V power supply. The MOSFET aspect ratios are given as: M1-M4 = 18μm/0.54μm, MA12-MA21 = 36μm/0.18μm, MA12-MA22 = 3.6μm/5.4μm, MA13-MA23 = 0.9μm/5.4μm, MA14-MA24 = 0.36μm/0.18μm. Capacitors C_Z and C_C are chosen to have values of 15 fF and 530 fF respectively to perform compensation scheme. Bias currents of I_b are taken as 10 μA. The minimum output
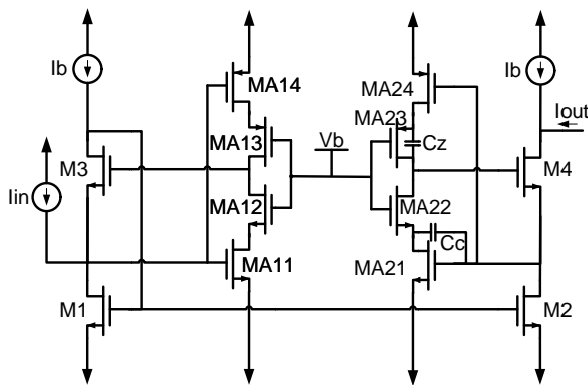
voltage is measured assuming that current mirror is working in class A. The result is illustrated in Fig. 4 which shows $V_{out,min}$ remains well below 0.18V. In the same condition the current copy error is measured as 0.003%. The current copy error is shown in Fig. 5 which shows that the current copy error favorably remains under 0.018% for currents up to 100 μA.

The excellent current transfer performance exhibiting both the very high accuracy and very wide current dynamic range is shown in Fig. 6. All other parameters are given at I_{bias} and compared with same ones of some other advanced works in Table .1. The output resistance is determined to be approximately 36.9GΩ. For a DC sweep of I_{in} from 1pA to 350μA, the maximum input voltage variation was found to be 0.002mV. This corresponds to an input resistance of approximately 0.0058 Ω (as is measured in [13], [15]). Fig. 6 shows the I_{out} in terms of I_{in} which proves the ultra wide dynamic range of the proposed current mirror. This is mainly due to much higher compliances, lower input and higher output impedances that help the circuit to preserve its linearity over applied wide range current. The total power consumption of the proposed current mirror is about 20μW. The capacitances included in Fig. 3 are not strictly for compensation. Actually as can be observed in Fig. 7(b) (dashed line), in absence of those capacitances an overshoot appears in frequency response. Although the overshoot amplitude is less than 0.8 dB which is much less than permitted value of 3 dB for overshoot, but for more reliability these capacitances are used to shift the
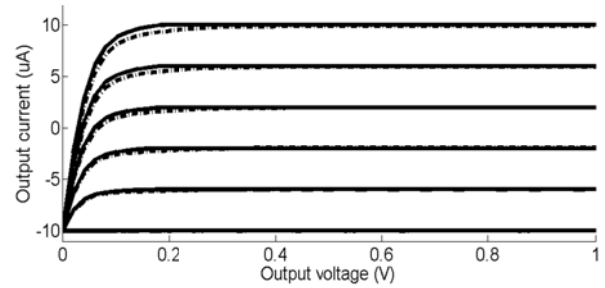

Fig. 4 DC Output characteristics Iout vs Vout; Vout swept from 0 to 1V; Iin varied from -10μA to 10μA in steps of 4μA. —) proposed. -.-.) LVCCM.
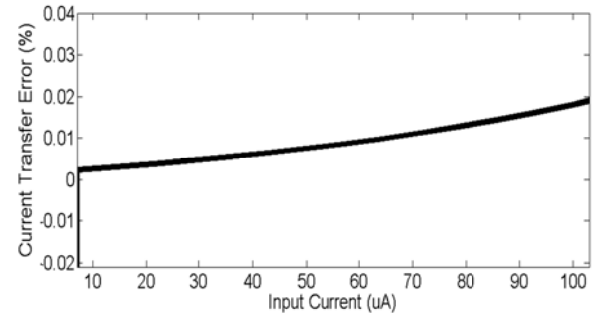

Fig. 5 Current transfer error of proposed circuit in terms of input current.

Fig. 3 Proposed current mirror utilized inverter as amplifier.

Table 1 The important parameters of the proposed current mirror compared with those of some other advanced works.

Ref.e	[10]Fig.2(a)	[11] Fig.4	[13]	[14]	[15]	[10] Fig.1(b)	[19] Fig.2(c)	This work
Rin (Ω)	27	33	0.75	0.01	0.012	20	~0.006	0.0058
Rout (GΩ)	NA	NA	0.2	10	2.3	0.039	0.407	36.9
P(μW)	341	218	NA	NA	NA	20	161	20
BW(MHz)	907	185	620	200	220	374	577	*240 & 166
Vdd (V)	1	1.5	1.8	3	1.8	1	1.5	1
Vin(V)	NA	NA	NA	NA	NA	0.30	0.7	0.18
Vout(V)	NA	NA	0.4	0.15	0.46	0.38	0.2	<0.18
I_{offset}	NA	830nA	NA	NA	NA	1nA	10pA	1pA
DR (dB)	NA	56.9	NA	NA	NA	42.6	NA	150
CTE** (%)	0.5	2.4	0.1	0.1	0.05	1.28$_{@ Iin=10\mu A}$	***-0.07,0,& 10μA	0.003$_{@ Iin=10\mu A}$
I_{bias} (μA)	50	50	110	50	25	10	50	10
CMOS Tech.(μm)	TSMC 0.18	TSMC 0.18	AMI 0.5	AMI 0.5	AMI 0.5	TSMC 0.18	TSMC 0.18	TSMC 0.18

* 240 without capacitances with 0.8dB over shoot and 166 with capacitances.

** Current transfer error

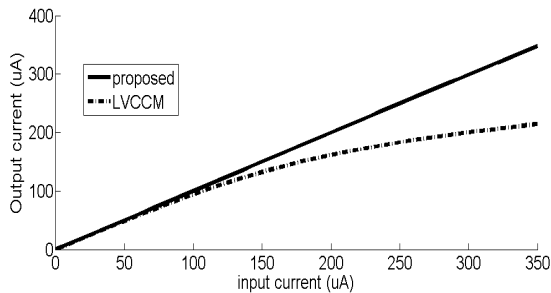*** -0.07 @ Ibias=50μa, min. Zero @ 55 μA, max.10 μA @ 250 μA

Fig. 6 Output current versus input one (DC transfer curve).

location of the existed double zero-pole pairs to remove the undesired overshoot as is shown in Fig. 7(a). The frequency response of the proposed current mirror is shown in Fig. 7 and exhibits -3dB frequency bandwidth of 166MHz. Although 166MHz is an acceptable frequency range but comparing with other similar reported works it is relatively small which is considered as one of the drawbacks of the current design. This degraded value for bandwidth is directly related to utilized amplifiers which include transistors with relatively large channel length to achieve higher gains (thus lower input and higher output impedances) and lower power consumption.

The amplifiers are considered as the main and most effective part of the proposed current mirror which their performance affect the overall performance of the circuit dominantly. Thus the PSRR analysis for amplifiers' gain is performed to study the rate of sensitivity of the amplifiers (thus the circuit) to the variations of VDD. Actually the presence of high gain amplifiers inside the feedback loop promises a satisfactory result. In other words, since amplifiers are incorporated in a closed feedback loop their performance should be highly desensitized against power supply variations [19] as is practically proved by

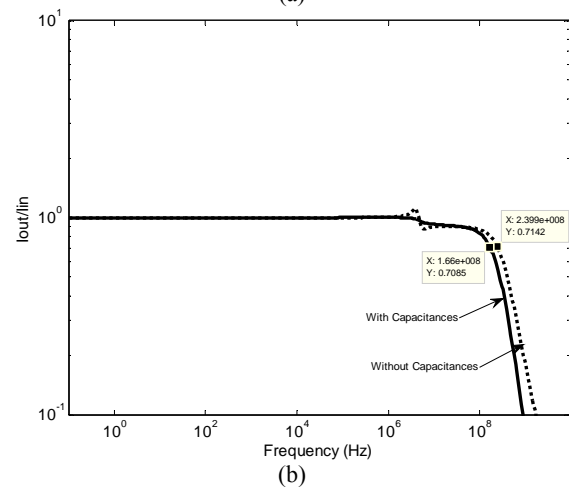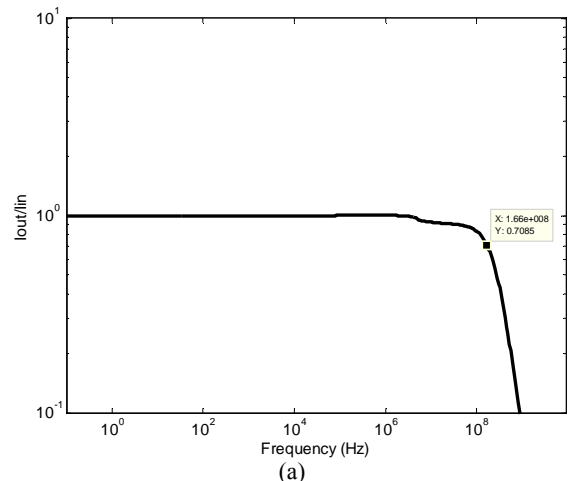high value of 65dB for the PSRR (as is defined in [19-20]) shown in Fig. 8.

(a)

(b)

Fig. 7 Frequency response of proposed current mirror: with capacitances (a) without capacitances (b, dashed line).
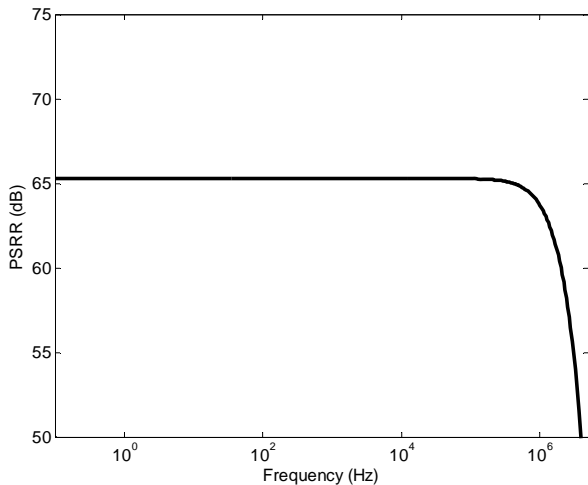
Fig. 8 PSRR of the amplifiers as the main and most important of the proposed current mirror

4 Conclusion

A Novel compact implementation of a very high performance low voltage low power current mirror is introduced and validated with HSPICE simulations. This circuit has extremely low input impedance, ultra high output impedance, high input and output compliance, very low power consumption, ultra high accuracy and ultra wide current dynamic range. The simulation results are performed using HSPICE TSMC 0.18μm CMOS, BSIM3 and Level49 technology with single 1 V power supply that verifies high performance of the introduced current mirror.

References

[1] Sharma S., Rajput S. S., Magotra L. K. and Jamuar S. S., "FGMOS based wide range low voltage current mirror and its applications", *2002 Asia-Pacific Conference on Circuits and Systems* (APCCAS '02), Vol. 2, pp. 331-334, 2002.

[2] Sharma S., Rajput S. S., Magotra L. K. and Jamuar S. S., "FGMOS Current Mirror: Behaviour and Bandwidth Enhancement", *Analog Integrated Circuits and Signal Processing*, Vol. 46, No. 3, pp. 281-286, 2006.

[3] Rajput S. S. and Jamuar S. S., "A Current Mirror for Low Voltage, High Performance Analog Circuits", *Analog Integrated circuits and signal processing*, Vol. 36, No. 3, pp. 221-233, 2003.

[4] Rajput S. S. and Jamuar S. S., "Advanced Current Mirrors for Low Voltage Analog Designs", *IEEE International Conference on Semiconductor Electronics (ICSE 2004)*, pp. 258-263, 2004.

[5] Azhari S. J., Faraji Baghtash H. and Monfaredi K., "A Novel Ultra High Compliance, High Output Impedance Low Power Very Accurate High Performance Current Mirror", *Microelectronics Journal*, Vol. 42, No. 2, pp. 432-439, 2011.

[6] Baghtash H. F., Monfaredi K. and Azhari S. J., "A novel high performance Atto-Ampere Current Mirror," *International Conference on Signal Acquisition and Processing,* pp. 27-30, 2010.

[7] Azhari S. J., Monfaredi K. and Baghtash H. F., "A Novel Ultra Low Power High Performance Atto-Ampere CMOS Current Mirror With Enhanced Bandwidth," *Journal of Electronic Science and Technology*, Vol. 8, No. 3, pp.251-256, Sept. 2010.

[8] Monfaredi K., Baghtash H. F. and Azhari S. J., "A novel low voltage current compensated high performance current mirror/NIC", *IEEE 11th Int'l Symposium on Quality Electronic Design*, pp.437-442, 2010.

[9] Rajput S. S. and Jamuar S. S., "Low Voltage Analog Circuit Design Techniques", *IEEE Circuits and Systems Magazine*, Vol. 2, No. 1, pp. 24-42, 2002.

[10] Gabbouj H. B., Hassen N. and Bsebes K., "Comparative study and design of new low voltage high performance current mirrors", *IEEE 3rd International Conference on Design and Technology of Integrated Systems in Nanoscale Era*, pp.1-6, 2008.

[11] Koliopoulos C., Psychalinos C., "A Comparative Study of the Performance of the Flipped Voltage Follower Based Low-Voltage Current Mirrors", *Signals, Circuits and Systems (ISSCS)*, Vol. 1, pp. 1-4, 2007.

[12] Ramírez-Angulo J., Carvajal R. G. and Torralba A., "Low Supply Voltage High-Performance CMOS Current Mirror With Low Input and Output Voltage Requirements", *IEEE Transactions on Circuits and Systems-II: Express Briefs*, Vol. 51, No. 3, pp.124-129, Mar. 2004.

[13] Ramirez-Angulo J., Sawant M. S., Lopez-Martin A. and Carvajal R. G., "Compact Implementation of High Performance CMOS current mirror", *Electronics Letters*, Vol. 41, No. 10, pp. 3-4, May 2005.

[14] Garimella A., Garimella L., Ramirez-Angulo J., Lopez-Martin A. J. and Carvajal R. G., "Low-voltage high performance compact all cascode CMOS current mirror", *Electronics letters*, Vol. 41, No. 25, pp. 1359-1360, 2005.

[15] Sawant M. S., Ramirez-Angulo J., Lopez-Martin A. J. and Carvajal R. G., "New Compact Implementation of a very High Performance CMOS Current Mirror", *IEEE 48th Midwest Symposium on Circuits and Systems*, Vol. 1, pp. 840-842, 2005.

[16] Carvajal R. G., Ramírez-Angulo J., López-Martín A. J., Torralba A., Gómez Galán J. A., Carlosena A. and Muñoz Chavero F., "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design", *IEEE Transactions on*

Circuits and Systems-I, Vol. 52, No. 7, pp. 1276-1291, Jul. 2005.

[17] Rodriguez-Villegas E. and Barnes H., "Solution to the trapped charge in FGMOS transistors", *Electronics Letters*, Vol. 39, No. 19, pp. 1416-1417, 2003.

[18] Rodriguez-Villegas E., Jimenez M. and Carvajal R. G., "On dealing with the charge trapped in floating-gate MOS (FGMOS) transistors", *IEEE Transactions on Circuits and Systems-II: Express Briefs*, Vol. 54, No. 2, pp. 156-160, 2007.

[19] Baghtash H. F. and Azhari S. J., "Very low input impedance low power current mirror", *Analog Integrated Circuits and Signal Processing*, Vol. 66, No. 1, pp. 9-18, 2011.

[20] Hassen N., Gabbouj H. B. and Bsebes K., "Low-voltage high-performance current mirrors: Application to linear voltageto-current converter", *International Journal of Circuit Theory and Applications*, Vol. 39, No. 1, pp. 47-60, 2011.

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