A New Low-Voltage, Low-Power and High-Slew Rate CMOS Unity-Gain Buffer

M. Piry*, M. Khanjanimoaf* and P. Amiri* (C.A.)

Abstract: Class-AB circuits, which are capable of dealing with currents several orders of magnitude larger than their quiescent current, are good candidates for low-power and high slew-rate analog design. This paper presents a novel topology of a class AB Flipped Voltage Follower (FVF) that has better slew rate and the same power consumption as the conventional class-AB FVF buffer previously presented in literature. It is thus suitable for low-voltage and low-power stages requiring low bias currents. These buffers have been simulated using 0.5 µm CMOS Technology models provided by IBM. The buffer consumes 16 µA from a 0.9 V supply and has a bandwidth of 52 MHz with an 18 pF load. It has a slew rate of 10.3 V/µs and power consumption of 36 µw.

Keywords: Class-AB Circuits, CMOS Integrated Circuits, Flipped Voltage Follower, High Slew Rate Buffers,Level Shifting Techniques.

1 Introduction

Voltage follower which is here denoted as VF, are widely used as output stages of opamps or in standalone configuration for signal conditioning, to accurately force an input voltage to an output load with both high input and low output impedance [1]. The conventional configuration of a VF is the voltage follower shown in Fig. 1-a. It has an output impedance of $R_{out} = 1/g_m$ (~ 2 kΩ) [2] and positive slew rate $SR = I_{D2}/C_L$. Notation C_L is the load capacitance, I_{D2}, the drain current of transistor M2 and g_m, the small signal transconductance.

This VF is biased on the source side with a constant current source (M2) which ideally keeps a constant gate-to-source voltage in M1. This causes output voltage variations to follow the input voltage with a gate to source DC level shift. In practice this VF suffers from some problems like, not enough low output impedance, dependence of drain current of M1 on I_{out} and nonsymmetrical slew rate.

The FVF [3] shown in Fig. 1-b is an improvement to a conventional VF. The FVF has a constant current through transistor M1, independent on the output current. Because of the shunt feedback [4], the output impedance is decreased to:

$$R_{out} = \frac{1}{\frac{1}{r_{o2}} + g_{m2}(1 + r_{o1} g_{m1})} \cong \frac{1}{g_m^2 r_o} \quad (1)$$

It is much smaller than R_{out} of conventional VF. The voltage gain is almost unity:

$$\frac{V_o}{V_i} = \frac{r_{o_1} r_{o_2} g_{m_1} g_{m_2}}{r_{o_1} r_{o_2} g_{m_1} g_{m_2} + r_{o_2} g_{m_2} + 1} \quad (2)$$

This is bigger than the voltage gain of conventional VF. The circuit in Fig. 1-b is able to source a large current but its sinking capability is limited by the drain current of M3.

To overcome this problem, circuit in Fig. 1-c [5-7] is used. Under quiescent conditions, every transistor is in saturation region and no current is delivered to the load. Neglecting second order effects, transistor M4 copies the drain current of transistor M1. Therefore the total current taken from the supply voltage is $2I_b$ (= $2I_{D3}$) which increases the power consumption of the circuit.

In this paper a very simple, low-voltage class-AB structure is proposed which is able to take current from supply sources only when the load requires it, so the power consumption decreases, and the slew rate increases, thus it can be used in low-voltage and low-power amplifiers as a level shifter [8].

The proposed structure has been simulated using the models of the IBM CMOS 0.5 µm technology, in order to compare its performance with the other buffers in terms of settling time, bandwidth, output impedance, power consumption and total harmonic distortion.

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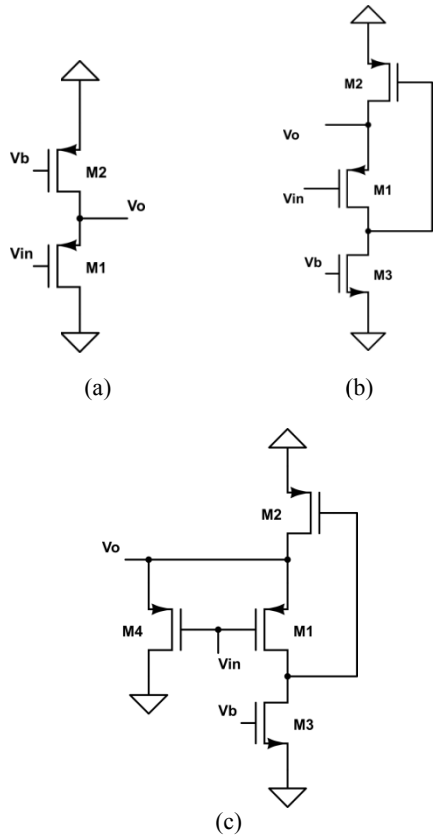


Fig. 1 Unity-Gain buffers: (a) Conventional VF. (b) FVF [3]. (c) Class-AB FVF [7].

2 A New Class-AB Unity Gain Buffer

The new unity-gain buffer in Fig. 2 is able to source and sink a maximum current which is larger than its quiescent current, as it will be shown next.

When the input signal V_{in} increases, with respect to the output voltage V_o, the source-to-gate voltage of transistor M1 tends to decrease. As transistor M1 is biased by the current source M3, its drain-to-source voltage rises, forcing a large current through transistor M2, and leading the transistor M4 into the cut-off region. In this operation regime the output current is I_{D2}-I_{D3}, and the output impedance is given by:

$$R_{out} = \frac{1}{\frac{1}{r_{o_2}} + g_{m_2}(1 + r_{o_1} g_{m_1})} \tag{3}$$

When the input signal decreases, the source-to-gate voltage of transistor M1 tends to increase and this transistor tends to the ohmic region. As the current through transistor M1 is fixed by M3, its source-to-drain voltage decreases, leading the transistor M2 into the cut-off region and transistor M4 into the saturation region. In this operation regime the current which is sinking equals to I_{D3}+I_{D4}, and the output impedance is approximately given by:

$$R_{out} = \frac{1}{\frac{1}{r_{o_4}} + g_{m_4}(1 + r_{o_1} g_{m_1})} \tag{4}$$

Thus transistor M4 sinks current only when the input signal decreases, so the current taken from the supply voltage in quiescent conditions is lower than FVF in Fig. 1-b.

In quiescent conditions, the gate-to-source voltage of transistor M4 is given by:

$$V_{GS_4} = V_{DD} - V_{SG_2} - V_{SS} = V_{DD} - \sqrt{\frac{I_{D_2}}{k_2}} - \left|V_{th_P}\right| - V_{SS} \tag{5}$$

In Eq. (5), k_2 is $\frac{1}{2}\frac{\mu_P C_{OX} W}{L}$. To keep the drain current of transistor M4 near zero, its gate-to-source voltage should be near the threshold voltage of transistor M4. Thus the Eq. (5) is given by:

$$V_{DD} - V_{SS} = V_{th_N} + \sqrt{\frac{I_{D_2}}{k_2}} + \left|V_{th_P}\right| \tag{6}$$

To decrease the required supply voltage, a DC level shifter shown in Fig. 3-a is used. In this circuit the Eq. (6) is given by:

$$V_{DD} - V_{SS} = V_{th_N} + \sqrt{\frac{I_{D_2}}{k_2}} + \left|V_{th_P}\right| - V_L \tag{7}$$

One basic implementation of this DC level shifter is shown in Fig. 3-b, in which VL is the source-to-gate voltage of transistor M5. The minimum voltage required to keep M1 in saturation is given by:

$$V_i \geq V_{G_2} - |\,V_{th_p}\,| \tag{8}$$

To keep M4 in saturation region, condition (9) should be satisfied:

$$V_i \geq V_{G_2} + V_L - V_{SG_1} - V_{th_N} \tag{9}$$

From Eqs. (8) and (9), we conclude that decreasing the input signal leads the transistor M1 into the ohmic region before the transistor M4.

If the input signal is a square wave, in the falling edge, the gate voltage of transistor M2 increases, this voltage is shifted to a higher value by transistor M5 and leads transistor M6 into the cut-off region. Fig. 4-a shows the variations of gate voltages of transistors M2 and M4. In Fig. 4-a a limitation can be observed as the gate voltage of transistor M4 cannot exactly follow the variations of gate voltage of transistor M2. Thus the maximum drain current of transistor M4 is limited, so the negative slew rate decreases.

A better technique for implementation of this floating voltage source is discussed in [9], shown in Fig. 3-c. In quiescent conditions, the gate voltage of transistor M4 is equal to V_C and the voltage across capacitor C is equal to $V_C - V_{G_2} = V_L$. Since the capacitor C and the resistor R form a high pass circuit with a

corner frequency $f_{3dB_{LOW}} = \frac{1}{2\pi RC}$, in order to set the lower 3 dB frequency as low as possible, resistor R should have extremely large values. Since typical values of integrated capacitors are in the pF range, to set $f_{3dB_{LOW}} < 100Hz$, R should be larger than 1 GΩ. Such a large resistor would have large area and parasitic capacitance that would limit the bandwidth of the amplifier. Efficient implementation of such a large resistor is discussed in [10], shown in Fig. 3-d. In this circuit, under dynamic conditions, only one of the transistors M5 and M6 are on, and the other is in cut-off region. So the equivalent resistance of the series combination of these transistors is very large. Under quiescent conditions the control voltages V_{b2} and V_{b3} keep M5 and M6 in sub-threshold region to have a very large effective resistance.

In the circuit of Fig. 3-d, the gate voltage variations of transistor M4 follow the gate voltage variations of transistors M2 exactly, as can be observed in Fig. 4-b. Thus this circuit overcomes the limitation mentioned before, and the negative slew rate is improved.

If we use the circuit in Fig. 3-d and its P-channel structure like the configuration shown in Fig. 5, although the power consumption increases, the slew rate improves, because the right circuit has the capability of sourcing large currents and the left one has the capability of sinking large currents, also transistors M4 and M10 improve the capability of sinking and sourcing current of right and left circuits respectively.

3 Simulation Results

The structures of proposed buffers (Fig. 3-d) and Fig. 5) and class-AB FVF [7] (Fig. 1-c) were simulated for comparison with V_{DD} = 0.45 V, V_{SS} = -0.45 V and C_L = 18 pF. For simulations 0.5 µm CMOS technology parameters provided by IBM (technology: SIGE05) were used that have nominal NMOS and PMOS threshold voltages V_{thN} = 0.67 V and $|V_{thP}|$ = 0.5 V respectively. The biasing current source is equal to 20 µA. All the devices used have 0.6 µm length. The sizes of transistors are reported in Table 1.

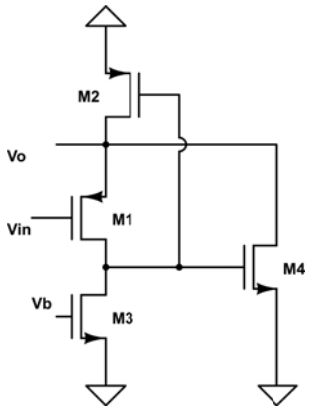


Fig. 2 Basic implementation of proposed circuit.

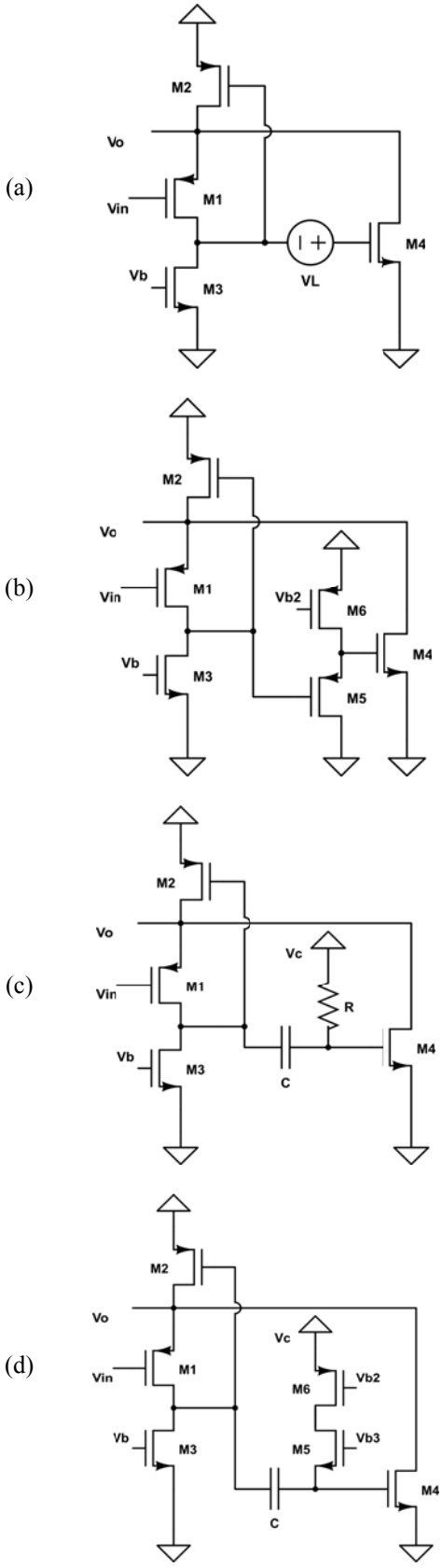
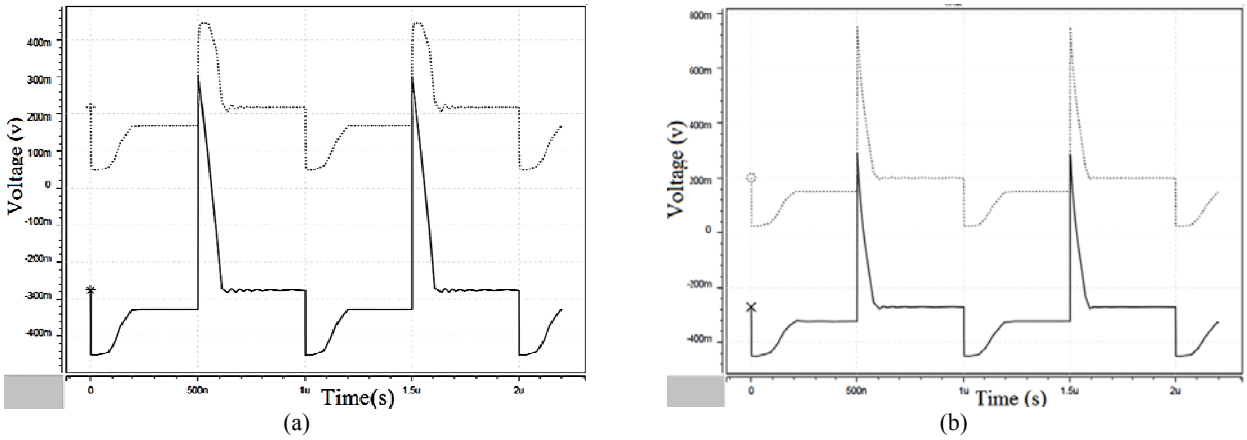


Fig. 3 Proposed circuit: (a) improved by level shifter. (b) DC level shifter implemented by transistor. (c) DC level shifter based on [10]. (d) large resistor implemented by transistor based on [10].



(a) (b)

Fig. 4 Gate voltage variations of transistors M2 (continuous line) and M4 (dotted line): (a) circuit 3(b). (b) circuit 3(d).

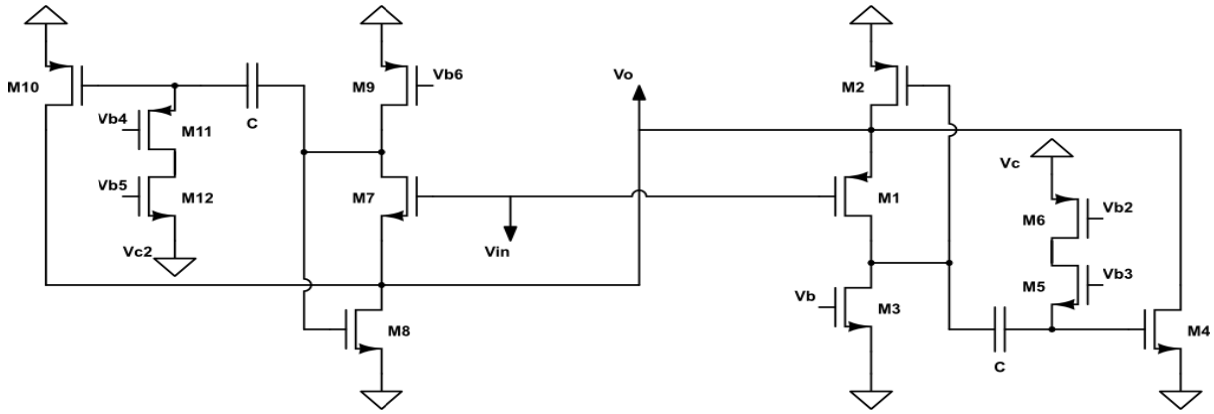


Fig. 5 Improved voltage buffer.

Fig. 6 shows the step response of the three buffers.The input step signals of the buffers have 400 mV_{PP} swing and frequency of 1 MHz. This figure shows the negative slew rate of 10.3 V/µs for the circuit of Fig. 5, 5.4 V/µs for the circuit of Fig. 3-d and 6.1 V/µs for the circuit of Fig. 1-c. That it agrees with the expected negative slew rate. Also the positive slew rate is 10.3, 2.7, 6.1 V/µs respectively.

Fig. 7 shows the frequency response comparison of all FVFs. They are characterized by similar 3 dB frequencies. It can be observed that the circuits have bandwidth of 51.5, 40.3 and 53.7 MHz respectively with a capacitor load of 18 pF.

Fig. 8 shows a comparison of the output impedance obtained by applying a 1 A AC current source to the buffer's output terminals with the input grounded. The voltage in this case corresponds exactly to the output impedance. It can be seen that the circuits have output impedance of 161, 299, 220 Ω respectively.

Fig. 9 shows the measured response for a 5 MHz, 200 mV peak-to-peak sinusoidal input voltage. The measured THD for a 1 MHz, 200 mV peak-to-peak sinusoidal input signal was -50.4, -45, -54.9 dB respectively.

In Fig. 10 the simulated output current for a 1 MHz, 200 mV square input signal is presented. The represented current is the one going through the load capacitor. It can be seen that the maximum current drained from load capacitor is 304, 251 and 217 µA and the maximum current sourced to the load capacitor is 550, 65 and 140 µA. It can be seen why the slew rate in the circuit of Fig. 5 is improved.

Fig. 11 shows the gain versus input voltage. It can be observed that the gain of second proposed circuit is constant in the larger input voltage range than the circuit of Fig. 1-c.

Table 1 Sizes of transistors.

MOS Width (µm)	Fig. 5	Fig. 3-d	Fig. 1-c
0.6	M5,M6,M11,M12	M5,M6	-
4	M3,M7	M3	M3
6	M4	M4	-
8	M2	M2	-
14	M1,M9,M8	M1	M1,M4
17	-	-	M2
70	M10	-	-

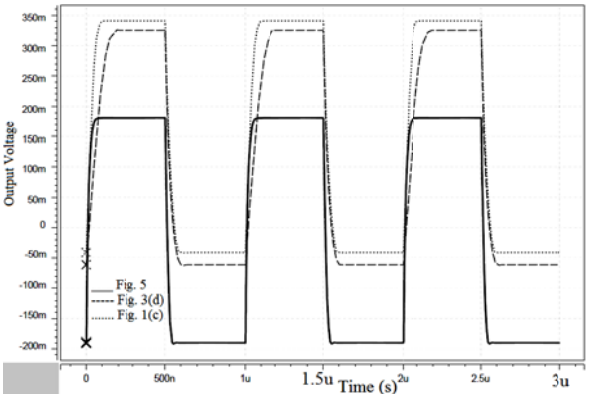


Fig. 6 Step response of three buffers.

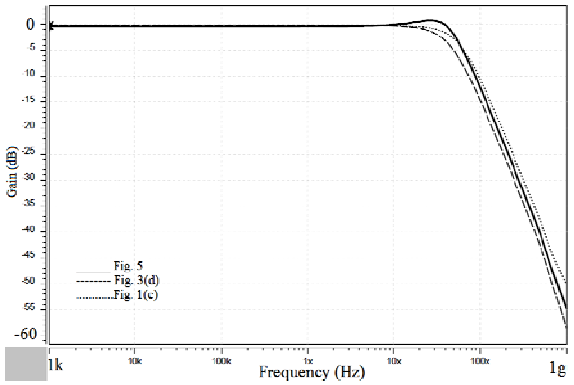


Fig. 7 Frequency response of buffers.

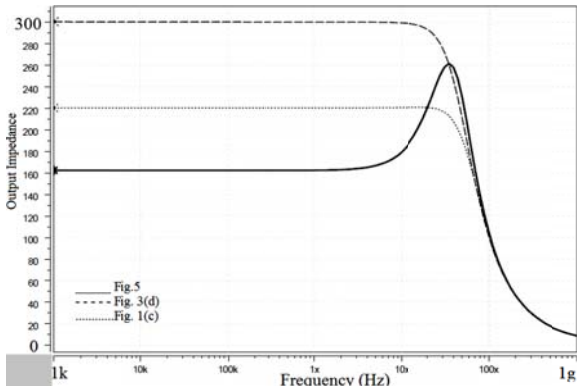


Fig. 8 Output impedance of buffers.

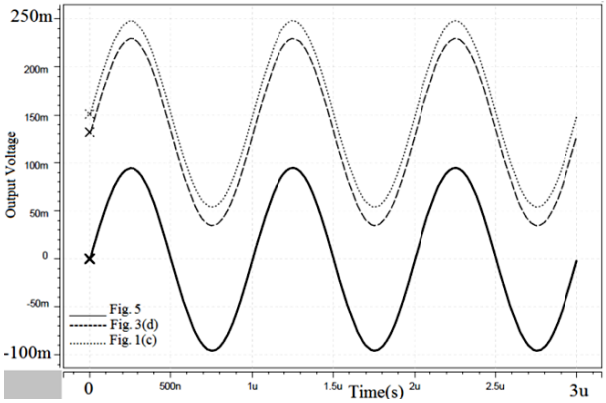


Fig. 9 Output of the buffers with 0.2 V_{PP} 1 MHz input.

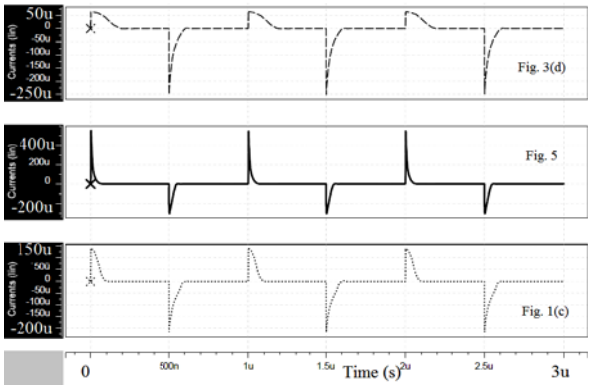


Fig. 10 Simulated output current with a 1 MHz 200 mV_{PP} square input signal.

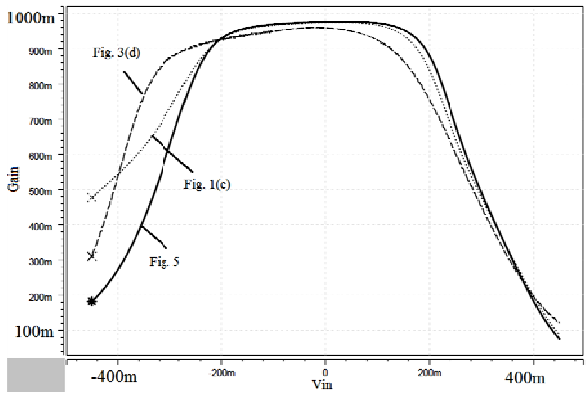


Fig. 11 DC gain of buffers vs. input voltage.

Note that the proposed buffers are rather stable under temperature variations: varying the temperature from -50 °C to 120 °C, the low-frequency gain varies by 0.1 dB for the second proposed circuit and varies by 0.01 dB for the first proposed circuit and class-AB FVF. The bandwidth is reduced from 77 MHz to 33 MHz and 68 MHz to 17 MHz for the second and the first proposed circuit respectively. While the bandwidth of class-AB FVF is reduced from 91 MHz to 27 MHz.

Since VLSI technology makes it possible to have mixed-signal circuits on a single die where digital circuits are integrated with analog blocks [11] and as the CMOS technology scales down [12, 13], noise analysis is critical subject for proposed circuits that will be performed in future.

4 Comparison of Buffers

Table 2 presents a comparison of buffers in terms of bandwidth, static power consumption, positive and negative slew rate, output impedance, voltage gain, THD, HD_2, HD_3 and FOM. Note that FOM is equal to (slew rate*C_L)/Power.

It can be seen that, although the power consumption in circuit of Fig. 5 is equal to the circuit of Fig. 1-c, the slew rate is highly improved. If we use circuit of Fig. 1-c in complimentary configuration like circuit of Fig. 5, although the slew rate enhances, the power consumption

increases to 72 µW, which is 30 µW larger than power consumption of circuit Fig. 5. Note that since in these circuits, transistors are operation in strong inversion they are not capable to operate under ultra-low-power application [13]. The bandwidth of second proposed circuit is larger than other buffer configurations presented in literature except the buffer Fig. 1-c. Thus it can be used in high frequencies. Also it can be seen that the second proposed circuit has the largest FOM among Fig. 3-d and Fig. 1-c.

5 Conclusion

A new class-AB unity-gain buffer based on the Flipped Voltage Follower (FVF) has been proposed. This circuit can be operated at a low voltage and low power. With respect to other class-AB stages based on the FVF topology, it has superior slew rate with low power consumption. This novel buffer has also low output impedance. The characteristics of the proposed circuit were validated by simulations.

Table 2 Comparison of buffers.

Circuit	Technology	Voltage Supply	I_D (µA)	P (µw)	BW	SR^+ (V/µs)	SR^- (V/µs)	FOM	R_{out} (Ω)	Gain (dB)	THD	HD_2 (dB)	HD_3 (dB)
Fig. 5 Second proposed circuit	0.5 µm	0.9 V	16	36	76 MHz C_L=10 pF	10.3	10.3	0.28	210	-0.35	-50 dB 200 mV_{PP} 1 MHz	-53	-54
Fig. 3-d First proposed circuit	0.5 µm	0.9 V	16	18	68 MHz C_L=10 pF	2.7	5.4	0.23	489	-0.2	-45 dB 200 mV_{PP} 1 MHz	-45	-60
Fig. 1-c Class-AB [7]	0.5 µm	1.5 V	20	36	87 MHz C_L=10 pF	6.1	6.1	0.17	220	-0.2	-55 dB 200 mV_{PP} 1 MHz	-56	-62
Buffer [1]	65 nm	1.2 V	10	-	100 MHz C_L=2 pF	-	-	-	760	-0.4	-	-	-
FVF [3]	65 nm	1.2 V	7.8	-	30 MHz C_L=2 pF	-	-	-	540	-0.6	-	-	-
SDP [5]	0.5 µm	3 V	30	-	11 MHz C_L=10 pF	-	-	-	2K	-	-59 dB 300 mV_{PP} 2 MHz	-	-
DFVF [5]	0.5 µm	3 V	30	-	70 MHz C_L=10 pF	-	-	-	40	-	-52 dB 300 mV_{PP} 2 MHz	-	-
CASDPFVF [5]	0.5 µm	3 V	30	-	70 MHz C_L=10 pF	-	-	-	0.5	-	-52 dB 300 mV_{PP} 2 MHz	-	-

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